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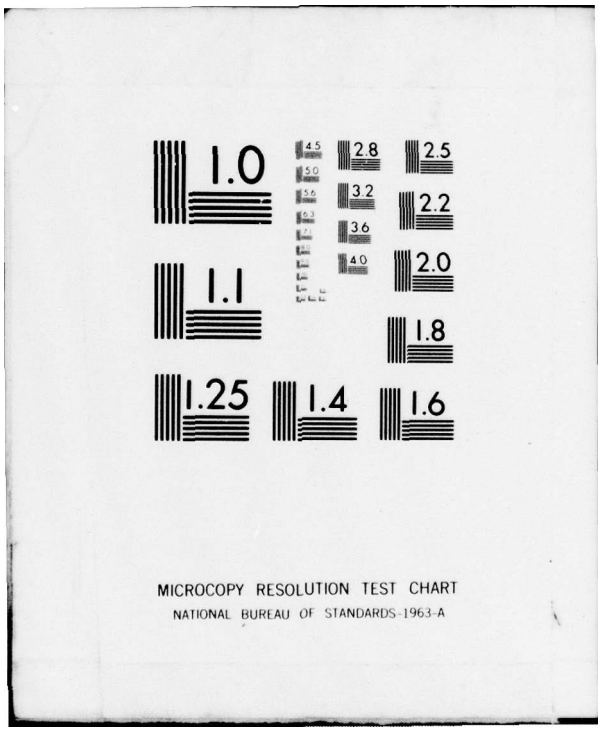
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NEUTRON HARDNESS ASSURANCE GUIDELINES FOR SEMICONDUCTOR DEVICES

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This guideline document develops a systematic approach to guarantee system survival at some specified probability of survival and neutron environmental level. The approach is analogous to a filtering process in which increasingly complex and costly levels of effort are applied until all system piece-parts have acceptable probabilities of survival. Branch decisions in the procedure are based on a statistical evaluation of manufacturer-to-manufacturer and lot-to-lot variations in piece-part neutron responses.

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Hardness assurance is part of the total quality assurance effort and includes all control, monitoring, and evaluation efforts needed to procure systems whose nuclear hardness equals or exceeds that of the design-hardened engineering prototype throughout production and system life. Hardness assurance efforts during the production phase are made part of the piece-part procurement specification. Example procurement specifications are given in this document for bipolar transistors, diodes, transistor-transistor logic integrated circuits, operational amplifiers (101A, 741, and 108A types), and junction-field effect transistors.

PREFACE

The concepts and procedures developed in this document evolved from an extensive effort by nuclear survivability/vulnerability specialists to establish a cost-effective set of guidelines for hardness assurance. This document has gone through several stages of development and the author is indebted to the following individuals who reviewed each draft: Joe Azarewicz, Jim Raymond, and Victor van Lint of Mission Research Corporation; Art Namenson and Al Wolicki of Naval Research Laboratories; Harvey Eisen of Harry Diamond Laboratories, Doug Millward of TRW, and George Messenger, consultant.

The intent of this document is to provide guidance to System Program Offices and their contractors to insure that nuclear design-hardened systems will meet their nuclear specifications throughout production and system life. This effort is defined as hardness assurance in AFSC Supplement 1 to AFR 80-38.[1] The guideline procedures set forth in this document conform to the hardness assurance plan developed by the Air Force.[2,3]

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[1]Air Force Regulation AFR 80-38, 6 September 1973, established requirements and responsibilities within the Air Force for conducting a nuclear survivability program.

[2]B-1 Hardness Assurance Guidelines, Aeronautical Systems Division, Wright-Patterson AFB, Ohio, Report ASD-TR-75-35, March 1976.

[3]Nuclear Hardness Assurance Guidelines for Systems With Moderate Requirements, Air Force Weapons Laboratory, Kirtland Air Force Base, NM, Report AFWL-TR-76-147, September 1976.

CONTENTS

CONTENTS (Con'd)

FIGURES

TABLES

1. INTRODUCTION

Systems which are to operate in a nuclear environment must be capable of nuclear survivability, which means they must be able to complete their mission in spite of nuclear stresses. The requirements and responsibilities within the Air Force for conducting a nuclear survivability program are given in Air Force Regulation 80-38.[1] Hardness assurance (HA) is defined as those control, monitoring, and evaluation efforts aimed at procuring systems whose nuclear hardness equals or exceeds that of the design-hardened engineering prototype.[2] In other words, HA addresses the problem of procuring parts for a system such that the system will be able to complete its mission when subjected to a predetermined nuclear radiation environmental level.

It is important to note that HA is done for a system that has already been designed to survive the specified radiation environment. Thus, HA is part of the total quality assurance effort and is carried out during the production phase of the system acquisition program. However, if the HA burden is placed entirely on part suppliers and procurement agencies, the result will be a substantial increase in part costs as these activities attempt to comply with very stringent procurement specifications. It is more cost effective to keep the number of parts requiring HA to a minimum by requiring the design activity to incorporate large design margins (overdesign) to relax procurement specifications whenever possible. This can be done, for example, by substituting a harder piece-part for a softer one. Thus, it can be seen that although HA is actually done during the production phase, it is very important to consider it in the design phase.

HA decisions are based on a statistical evaluation of the variation in unit-to-unit radiation responses that occur among the thousands of

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[1]Air Force Regulation AFR80-38, 6 September 1973, established requirements and responsibilities within the Air Force for conducting a nuclear survivability program.

[2]B-1 Hardness Assurance Guidelines, Aeronautical Systems Division, Wright-Patterson AFB, Ohio, Report ASD-TR-75-35, March 1976.

piece-parts that compose modern complex military systems. This guideline document develops a systematic approach to guarantee system survival at some specified probability of survival and radiation environmental level. This systematic approach is given in the flowchart of figure 1 and is based on a successive elimination of piece-parts with acceptable probabilities of survival. In this way the approach is analogous to a filtering process in which increasingly complex and expensive levels of effort are applied until all piece-parts have acceptable probabilities of survival to the given neutron environment.

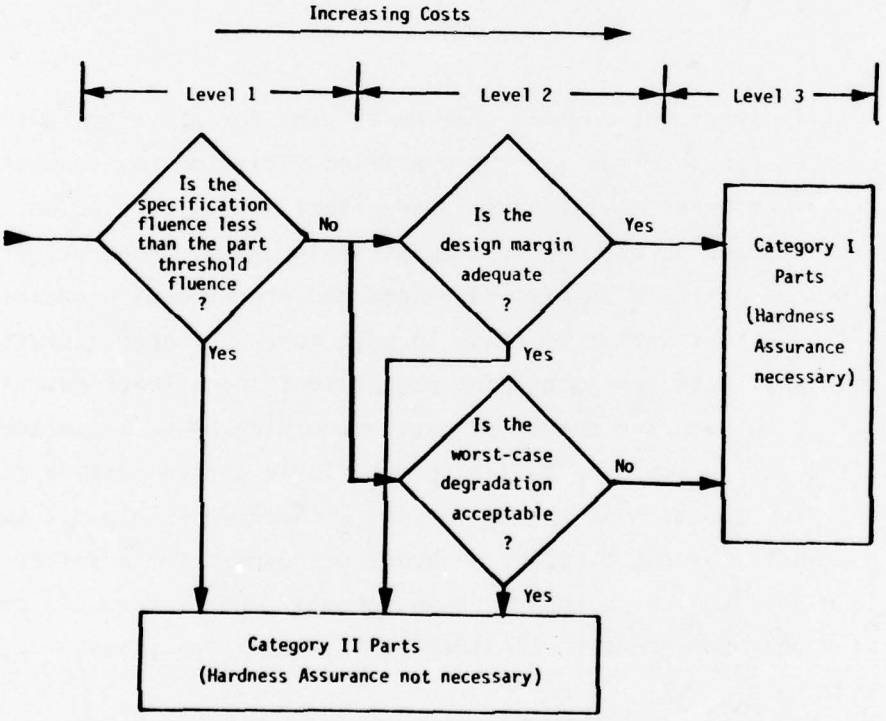

Figure 1. Neutron hardness assurance guideline procedure flow diagram.

The simplest way to obtain piece-parts with acceptable probabilities of survival is to select those parts with a threshold neutron damage fluence (Φ_{TH}) above the specification fluence (Φ_{SPEC}), as is indicated by level 1 in figure 1. As long as $\Phi_{SPEC} \leq \Phi_{TH}$, HA is not necessary and the part is labeled in all system documentation as category II.[3] Φ_{TH} is calculated from a device model by assuming the worst parameters that could possibly be encountered in a generic part type. This threshold concept and the accompanying calculations are discussed fully in section 2.1.

If Φ_{SPEC} is above Φ_{TH}, then the second level in the flowchart in figure 1 is encountered. At level 2 the determination of whether or not a piece-part is category II is accomplished by one of two methods: (1) from meeting an adequate design margin which is determined from a historical statistical characterization of variations in generic part type radiation response or (2) from a worst-case model calculation using measured device parameter values as an input. The determination of which method to use is based on the availability of needed information: the lack of a significant data base precludes the use of the statistically-derived design margin, and the lack of an adequate model precludes the use of the worst-case calculation. If either method indicates that the fluence at which the part will fail to perform its required function (Φ_F) at some specified probability of failure (P_F) is above Φ_{SPEC}, then the part is designated category II and no further action is required. If, however, Φ_F is below Φ_{SPEC} then level 3 in figure 1 is encountered.

Piece-parts reaching level 3 in the flowchart in figure 1 are those parts which are identified in all system documentation as category I parts.

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[3]The category I and II identification was originally defined by R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines for Systems with Moderate Requirements, Air Force Weapons Laboratory, Kirtland Air Force base, NM, AFWL-TR-76-147, September 1976.

Category I parts require control, monitoring, and evaluation efforts. Controls are placed on the part production processes to limit parameter variations. The monitoring effort encompasses all testing, screening, and lot-sampling. The evaluation effort applies the experience gained from the imposition of the control and monitoring efforts to HA methodology improvements.

A guideline methodology following the flowchart of figure 1 is developed in the body of this document using silicon bipolar transistors as an example. The methodology is applied to the following silicon devices in the appendices:

a. Reference diodes

b. Transistor-transistor logic (TTL) digital integrated circuits (IC's)

c. Operational amplifiers (LM101A, LM108A, and 741)

d. Junction field effect transistors (JFET's).

2. HARDNESS ASSURANCE REQUIREMENTS

In this section the levels of HA methodology illustrated in figure 1 are applied to transistors to illustrate the concept. Section 2.1 briefly describes the effects of neutron radiation in silicon bipolar transistors, discusses a theoretical worst-case model, and calculated a theoretical Φ_{TH}. Section 2.2 explains the design margin concept. Section 2.3 identifies HA procedures for category I parts.

2.1 Neutron Fluence Thresholds

Neutron radiation degrades the electrical characteristics of semiconductor devices by increasing the number of trapping, scattering, and recombination centers. Trapping centers remove majority carriers from the

conduction process, scattering centers reduce carrier mobility, and recombination centers decrease minority carrier lifetime.

The electrical performance of bipolar devices depends critically on sufficient minority carrier lifetime; thus, a decrease in this parameter due to neutron damage will significantly affect device performance by causing a transistor current gain (h_{FE}) decrease. The degradation of transistor reciprocal gain is linear with neutron fluence for moderate collector current levels where current crowding is not a problem and is given by[4]

$$1/h_{FE(RAD)} = 1/h_{FEO} + \frac{K}{2\pi f_T} \Phi \qquad (1)$$

where $h_{FE(RAD)}$ is the gain after neutron irradiation

h_{FEO} is the gain before neutron irradiation

K is the average lifetime damage constant ($cm^2/n \cdot s$)

Φ is the 1 MeV equivalent neutron fluence (n/cm^2)

f_T is the gain-bandwidth product (s^{-1}).

An approximate value for K at room temperature for a typical silicon transistor operated at a collector current near the maximum h_{FE} point is 0.8×10^{-6} $cm^2/n \cdot s$.[5] This is an average value for K; it needs to be derated for different collector current operating levels (K is a weak function of the type of impurity and resistivity for the range of resistivities commonly found in devices). If the collector current is one-tenth that of the maximum h_{FE} point, K should be increased to 2×10^{-6}; if the collector current is one-hundredth that of the maximum h_{FE}, point K should be increased to 7×10^{-6} $cm^2/n \cdot s$.[6]

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[4]G. Messenger and J. Spratt, The Effects of Neutron Irradiation on Germanium and Silicon, Proc. IRE, 1038, June 1958.

[5]B. Gregory and C. Gwyn, Application of Neutron Damage Models to Semiconductor Device studies, IEEE Trans. Nucl. Sci., NS-17, 325, December 1970.

[6]O. Curtis et al., Radiation Effects in Silicon and Germanium, Northrop Corporation, Los Angeles, CA, ARD-66-56R, August 1966.

The value for K also needs to be derated for neutron damage annealing. If a transistor must operate within one-tenth of a second after a neutron burst, K should be increased by a factor of two.[7] If the device need not operate until one second after the neutron burst, no correction factor for K is required.

K is a strong function of neutron energy. The K factor values listed above were obtained by converting neutron spectra to 1 MeV equivalent neutron fluence (silicon). This requirement will be discussed in section 3.

Transistor neutron damage is usually expressed in terms of a neutron damage factor (K_D) which is related to K by

$$K_D = \frac{K}{2\pi f_T} \quad .$$

A transistor model, discussed in appendix A, was developed in this program to calculate a worst-case value of K_D given the knowledge of the collector current operating point and electrical parameter specifications from the manufacturer's data sheet.[8] The threshold neutron fluence (discussed in section 1) for transistors can be calculated from this model by postulating the worst-neutron sensitive transistor that could be encountered. This worst-case transistor would have the following parameter values.

a. collector current ≤ 1 μA

b. base width ≥ 10 μm

c. emitter-base breakdown voltage ≤ 4 V

d. collector-base breakdown voltage ≥ 90 V

e. emitter area $\geq 4 \times 10^{-4}$ cm^2.

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[7]H. Sander and B. Gregory, Transient Annealing in Semiconductor Devices Following Pulsed Neutron Irradiation, IEEE Trans. Nucl. Sci., NS-13, 53, December 1966.

[8]A. Hart, et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, IEEE Trans. Nucl. Sci., NS-25, December 1978.

Assuming that a 1 percent change in $\Delta 1/h_{FE}$ ($\Delta 1/h_{FE}$ is equal to $1/h_{FE(RAD)} - 1/h_{FEO}$) is insignificant, the threshold fluence calculated from these values by the worst-case model is 1×10^{10} n/cm^2. The implication of this calculation is that transistors and IC's with transistors as component parts will not suffer any significant degradation at neutron fluences of 1×10^{10} n/cm^2 or below.

2.2 Design Margins

For a given device, the design margin is the factor relating the predicted failure level to the specification level for a particular nuclear environment.[3] The degree of control necessary for production parts acquisition is directly relatable to the design margin. If a substantial margin has been incorporated, then no controls will be needed. In other words, a design margin is used so that variations in piece-part parameters from lot to lot and manufacturer to manufacturer will not cause circuit failure.

In this document, the design margin relating the device mean neutron failure fluence (Φ_{MF}) to the specified neutron fluence (Φ_{SPEC}) will be defined as the neutron design margin (NDM). Its value is calculated by examining the statistical lot-to-lot and manufacturer-to-manufacturer variations in piece-part neutron responses. The statistical methodology used in making this calculation is presented in section 3.

Given the NDM and Φ_{SPEC}, level 2 in the flow chart in figure 1 shows that HA procedures can be avoided (category II criteria) by selecting a piece-part with a Φ_{MF} such that

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC} \qquad (3)$$

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[3] R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines for Systems with Moderate Requirements, Air Force Weapons Laboratory, Kirtland AFB, NM, AFWL-TR-76-147, September 1976.

where Φ_{MF} is the mean fluence at which the part will fail to perform its required function. For transistors, Φ_{MF} is found from equation 1:

$$\Phi_{MF} = \frac{2\pi f_T}{K}\left[1/h_{FE(FAIL)} - 1/h_{FEO}\right]$$

where $h_{FE(FAIL)}$, the circuit failure gain, replaces $h_{FE(RAD)}$. Replacing f_T and h_{FEO} with the minimum values from manufacturer's data sheets yields a minimum estimate of Φ_{MF},

$$\Phi_{MF} \gtrsim \frac{2\pi f_{T(MIN)}}{K}\left[1/h_{FE(FAIL)} - 1/h_{FE(MIN)}\right] \qquad (4)$$

where K is the average value of 0.8×10^{-6} $cm^2/n \cdot s$ discussed earlier for collector currents near maximum h_{FE}. The procedure for calculating the NDM will be covered in section 4.1.

By substituting the numbers for a particular transistor into the above equations, a minimum estimate of Φ_{MF} divided by the NDM can be calculated and compared to Φ_{SPEC}. If it is larger than Φ_{SPEC}, the device is category II and HA controls are not necessary. If it is smaller than Φ_{SPEC}, the device is category I and HA controls are encountered.

2.3 Category I Hardness Assurance Requirements

HA controls and monitoring efforts for category I parts can be divided into two control levels: control level 1 (S-1) calls for the HA techniques of process controls, 100 percent non-degrading screens, and radiation lot-sample testing; control level 2 (S-2) calls for process controls and electrical screens, but not radiation testing.

Category I parts should be drawn from the most homogeneous population available. A ranking of production populations in order of decreasing homogeneity is

a. wafer

b. wafer lot

c. diffusion lot

d. metallization lot (including passivation)

e. production lot (dicing and packaging)

f. date code (date when testing was done)

g. one manufacturer

h. hi-rel devices from different manufacturers

i. different manufacturers.

The lowest traceable cost level is the date code. The desired traceable level for neutron response, however, is the diffusion lot. The problem is that traceability is lost at the dicing step (production lot), unless relatively expensive records and markings are maintained. The recommended first step is, therefore, to obtain category I parts from one date code. If the date code parameter variations are too large, then diffusion lots must be procured.

As one proceeds up the above population list the available sample size is reduced. This means that part variations must narrow faster than the available sample size for lot-sample statistical control to have any meaning. This will become more evident when statistical lot-sampling techniques are discussed in section 3.

The decision to impose S-1 or S-2 controls is based on the cost-effectiveness of an electrical screen. Practically any parameter that can be correlated to some degree with radiation can be used as an HA screen; however, only cost-effective screens should be used.

The contractual vehicle by which HA techniques are imposed is the procurement specification; an example is given (for the 2N2222 transistor) in table I. The procurement specification should list HA control and monitoring effects, the parameters to which these efforts are applied, the test methods and test conditions, and the accept/reject failure criteria. The radiation quality conformance lot-sample tests are read-and-record tests on 5 to 20 samples at three neutron levels that cause 20, 50, and 80 percent degradation in $1/h_{FE}$.

TABLE I. PROCUREMENT SPECIFICATION EXAMPLE (2N2222) FOR CATEGORY I PARTS

Hardness assurance control	Parameter	Test method	Test condition	Control level failure criterion S-2 Min	S-2 Max	S-1 Min	S-1 Max	Units
Process controls	Base width and resistivity profile	TBD	TBD	-	TBD	-	TBD	TBD
	Configuration	TBD	TBD	-	-	-	-	-
Screens	$h_{FE(MIN)}$	MIL-STD-750B-3076.1	I_C = 10 mA	75	-	75	-	-
	$f_{T(MIN)}$	MIL-STD-750B-3306	I_C = 10 mA	250	-	250	-	MHz
Radiation quality conformance test	K_D	MIL-STD-883B-1017	I_C = 10 mA	-	-	-	TBD	cm^2/n

NOTES: TBD means to be determined. The test methods are from MIL-STD-750B, Test Methods and Procedures for Semiconductor Devices. The parameters h_{FE}, f_T, I_C, and K_D are the common emitter current gain, gain-bandwidth product, collector current, and neutron damage factor, respectively.

Process controls should be specified and maintained by the manufacturer for control levels S-2 and S-1. The idea is not to put tight tolerance limits on the manufacturer so that a significant number of parts are rejected, but merely to call for the specification and the maintenance of any neutron-sensitive parameter to reduce lot-to-lot variability in the radiation response of the device. Process-related parameters that contribute to K_D and hence require controls are the base width, base doping, emitter area, and collector doping. A sensitivity analysis reduces this list to base width and base doping.[8] Effects on K_D from variations in emitter area and collector doping are generally less than the effects produced by varying the base width and base doping for devices not operated at high currents. For this reason, process controls for transistors should consist of controls on the base width and the base resistivity profile.

The transistor terminal electrical parameters that correspond to the four physical parameters above, and hence are good screening candidates, are the minimum f_T, minimum emitter-base breakdown voltage, maximum input capacitance, and minimum collector-base breakdown voltage. For transistors operated as small-signal amplifiers, the most effective electrical screens are on $h_{FE(MIN)}$ and $f_{T(MIN)}$.

The important process controls for neutron degradation and their related terminal parameters are thus:

Process controls	Terminal parameters that monitor process controls
Upper bound base width	Minimum gain bandwidth product
Upper and lower bounds on base doping	Minimum emitter-base breakdown voltage
	Minimum collector-base breakdown voltage
Upper bound on emitter area	Maximum input capacitance

[8] A. R. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, IEEE Trans. Nucl. Sci., NS-25, December 1978.

3. RADIATION TESTING AND DATA ANALYSIS

Neutron radiation test procedures, facilities, and dosimetry needed to produce lot-sample data required for acceptance of S-1 devices are discussed in this section. In addition, a statistical methodology is presented for radiation data analysis and NDM calculations.

3.1 Radiation Testing

A radiation test plan is necessary to specify the details of preirradiation and postirradiation electrical measurements, neutron test levels, and neutron dosimetry. Except for dosimetry, test details vary from device to device. In this section, only the common test requirements for all devices are addressed.

In order to establish a good neutron data base, it is important to follow the same test procedures. A standard method for these test procedures was published on 31 August 1977 with the addition of the Neutron Irradiation Test Method 1017 to MIL-STD-883B.[9]

The most common neutron radiation sources are TRIGA's or fast burst reactors operating in either a pulse or a steady state mode. For this discussion, we assume that a TRIGA reactor is used, unless otherwise stated.

After preirradiation electrical tests are made, the devices are mounted in a holder usually with the leads shorted. The devices are irradiated in an unbiased mode because effects of bias during neutron radiation are usually small. The devices should be mounted in the holder

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[9]Test Methods and Procedures for Microelectronics, MIL-STD-883B. All MIL-STD documents are available from the Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.

so that the variation of fluence over the sample area does not exceed 20 percent. This is important because a 20 percent variation can occur in less than 20 cm in some reactors.

An example of in-core specifications for a TRIGA reactor follows:*

Thermal neutrons	1×10^7 n/(cm^2•s•W)
Neutrons above 10 keV	2×10^7 n/(cm^2•s•W)
Gamma (γ) radiation	0.06 rad/(s•W)

The amount of TRIGA time needed to get 1×10^{12} n/cm^2 can be calculated as follows. Assume that with cadmium-lined sample holders in-core, the reactor power level is set at 1 kW. The neutron flux for neutrons above 10 keV is thus

$$(2)(10^7)\frac{n}{cm^2 \cdot s \cdot W}\ (10^3\ W)(60) = (1.2)(10^{12})\frac{n}{cm^2 \cdot min}$$

or the desired fluence is obtained in about 1 min. Higher fluences can be achieved in a reasonable amount of time by operating the reactor at higher power levels (up to ~1 MW for some TRIGA's). Cadmium can be used as a thermal neutron shield. The amount of attenuation, I, is approximated by

$$I = I_o e^{-155d}$$

where d is the cadmium thickness in centimeters. A 0.020-inch-thick cadmium shield attenuates the thermal neutrons by about a factor of 2.5×10^3. Thus, thermal neutrons are reduced from 1×10^7 to 4×10^3 n/(cm^2•s•W).

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* Reactor engineers sometimes use the term "NV", which is equivalent to neutrons/cm^2•s.

The gamma dose that accompanies the neutrons can be a problem, especially when testing linear IC's. It is usually desirable to obtain the highest neutron-to-gamma ratio possible to separate the effects of the two different types of radiations. The in-core TRIGA neutron-to-gamma ratio is approximately

$$\frac{(2)(10^7)}{0.06} = 3 \times 10^8 \text{ n/(cm}^2\text{rad)}$$

or a neutron-to-photon ratio of about 0.1, assuming an average photon energy of 1 MeV and using a 2×10^9 MeV/cm^2•rad conversion factor. Thus, every neutron is accompanied by about 10 photons.

The use of a TRIGA with a dry room reduces the fluence available by about 10^3 (to $\sim 4 \times 10^4$ n/cm^2•s•W). At a reactor power of 20 kW, the 10^{12} fluence is reached in about 20 minutes. The dry room has a higher neutron-to-gamma ratio of about 5×10^9 n/(rad•cm^2) with 4 inches (5.00 cm) of lead. About 1/2 inch (1.27 cm) of Boral is usually added to reduce the thermal neutrons. The White Sands Missile Range, Albuquerque, NM fast burst reactor has a similar neutron-to-gamma ratio (8×10^9) with 4 inches (10.16 cm) of lead.

Electrical tests are performed after exposure. Neutron-irradiated parts are radioactive, so postneutron tests may have to be delayed or made in situ. Integrated circuit dual in-line packages exposed to 10^{13} n/cm^2 can read 200 mR per hour (at 1 cm) after 15 minutes, 10 mR per hour after 4 hours, and 1 mR per hour after 10 days. These numbers vary widely from device to device and are used only to illustrate the problems in postneutron testing. All postneutron tests should be performed after clearance by the health physicist at the test facility.

Radiation facilities for performing military qualification tests should be certified. The basic requirements are set forth in MIL-STD-976.[10] The additional detailed requirements needed for radiation test facility certification include neutron dosimetry techniques, fluence levels, pulse lengths, methods for characterizing neutron spectra, and other items.

Neutron test data on semiconductor devices should be expressed in terms of neutrons per square centimeter (1 MeV silicon equivalent). A recent study of the most commonly used neutron facilities in the United States has led to the following set of ASTM draft standards:[11]

E10-07-78-1 Method for Irradiating a Standard Set of Neutron Threshold Activation Foils for Radiation Hardness Testing,

E10-07-78-2 Method for measuring Neutron Activated Foils for Radiation Hardness Testing,

E10-07-78-3 Recommended Practice for Measuring the Relative 1 MeV Silicon Equivalent Fluence.

In this study it was shown that the 1 MeV silicon equivalent neutron fluence is roughly 10 percent higher than the fluence obtained for neutrons of energy greater than 10 keV (non-thermal neutrons) for most facilities.

Common dosimetry equipment at reactors consists of sulfur pellets to measure the neutron fluence and CaF_2:Mn thermoluminescent dosimeters (TLD's) to measure the accompanying gamma dose. Lithium fluoride TLD's should not be used in a reactor environment. CaF_2:Mn TLD neutron sensitivity is about 2×10^{-17} rads$\cdot$cm^2/n, so they are relatively insensitive to neutrons.

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[10] Certification Requirements for JAN Microcircuits, MIL-STD-976, August 1977.

[11] V. Verbinski et al., Simultaneous Neutron Spectrum and Transistor Damage Measurements in Diverse Neutron Fields: Validity of $D_{Si}(E_n)$, Naval Research Laboratory, Washington, D.C., NRL Memorandum 3929, March 1979. The draft ASTM standards are not yet available; for information, contact the ASTM, 1916 Race Street, Philadelphia, PA 19103.

3.2 Statistical Data Analysis Procedure

In the introduction it was stated that HA is a probabilistic endeavor because of variations in unit-to-unit radiation response. In this section the statistical procedures for evaluating radiation test lot-sample data are discussed (radiation testing is a destructive test so lot-sample statistics are required). Two important conditions are made:

a. Since sample sizes are limited, a variable sampling plan (as opposed to an attribute sampling plan) is required to permit statistical extrapolation to required low probabilities of failure.

b. The statistical distribution of the radiation test data is assumed to be lognormal (the natural logarithms of the parameter fit a normal distribution).

The first condition is made because of the large number of piece-parts that typically occur in modern electronic systems. It is not uncommon to find 1000 to 100,000 piece-parts in a complex system; when this occurs the failure budget for the individual piece-parts must be very low. For example, a system with a probability of success requirement of 90 percent and 1000 piece-parts will require a piece-part probability of failure (P_F) of 0.1/1000 or 1×10^{-4}. To attain this P_F at 90 percent confidence, using an attribute plan would require a sample size of over 2000 units.[12] Clearly this is unrealistic; a much smaller sample size must be used and extrapolated to the low probabilities of failure required by assuming the shape of the distribution.

The second condition is made because it is necessary to extrapolate small sample statistics out to the low probability of failures required for individual piece-parts. Is this assumption valid? A large number of

[12]General Specifications for Microcircuits, MIL-M-38510D, Appendix B, Lot Tolerance Percent Defective (LTPD) Plan.

transistors have been subjected to neutron irradiation in the past. Examination of this data bank has revealed that the data is either lognormal or closely approximated by a lognormal distribution.

In order to illustrate the statistical procedures for evaluating radiation test lot-sample data, consider the ten sample 2N2222 transistor data in table II. The value of h_{FE} at a collector current of 10 mA and a collector-emitter voltage of 5 V was measured before and after irradiation at 2.5×10^{13} n/cm^2. From the h_{FE} degradation data the K_D was calculated using (from equations 1 and 2)

$$K_D = \Delta(1/h_{FE})\frac{1}{\Phi} . \qquad (5)$$

The natural logarithms of the data ($\ell n\ K_D$) were then made. The $\ell n\ K_D$ data can be plotted on normal probability paper as in figure 2, where the cumulative percentage points on the vertical scale are found from 1/(N+1), 2/(N+1), 3/(N+1)...N/(N+1), where N is the sample size (10 in this case).

TABLE II. RADIATION LOT-SAMPLE DATA FOR TEN 2N2222 TRANSISTORS MEASURED WITH A COLLECTOR CURRENT OF 10 MILLIAMPS AND A COLLECTOR-EMITTER VOLTAGE OF 5 VOLTS

Preirradiation gain (h_{FEO})	$h_{FE(RAD)}$ at 2.5×10^{13} n/cm^2	Neutron damage factor (K_D) ($\times 10^{-16}$)	$\ell n\ K_D$	Cumulative distribution (percent)
146	78	2.31	-36.00	9.1
166	85	2.30	-36.01	18
151	84	2.11	-36.09	27
147	84	2.04	-36.13	36
200	100	2.00	-36.15	45
188	100	1.87	-36.22	54
220	111	1.79	-36.26	64
178	100	1.75	-36.28	73
160	96	1.67	-36.33	82
241	125	1,34	-36.41	91

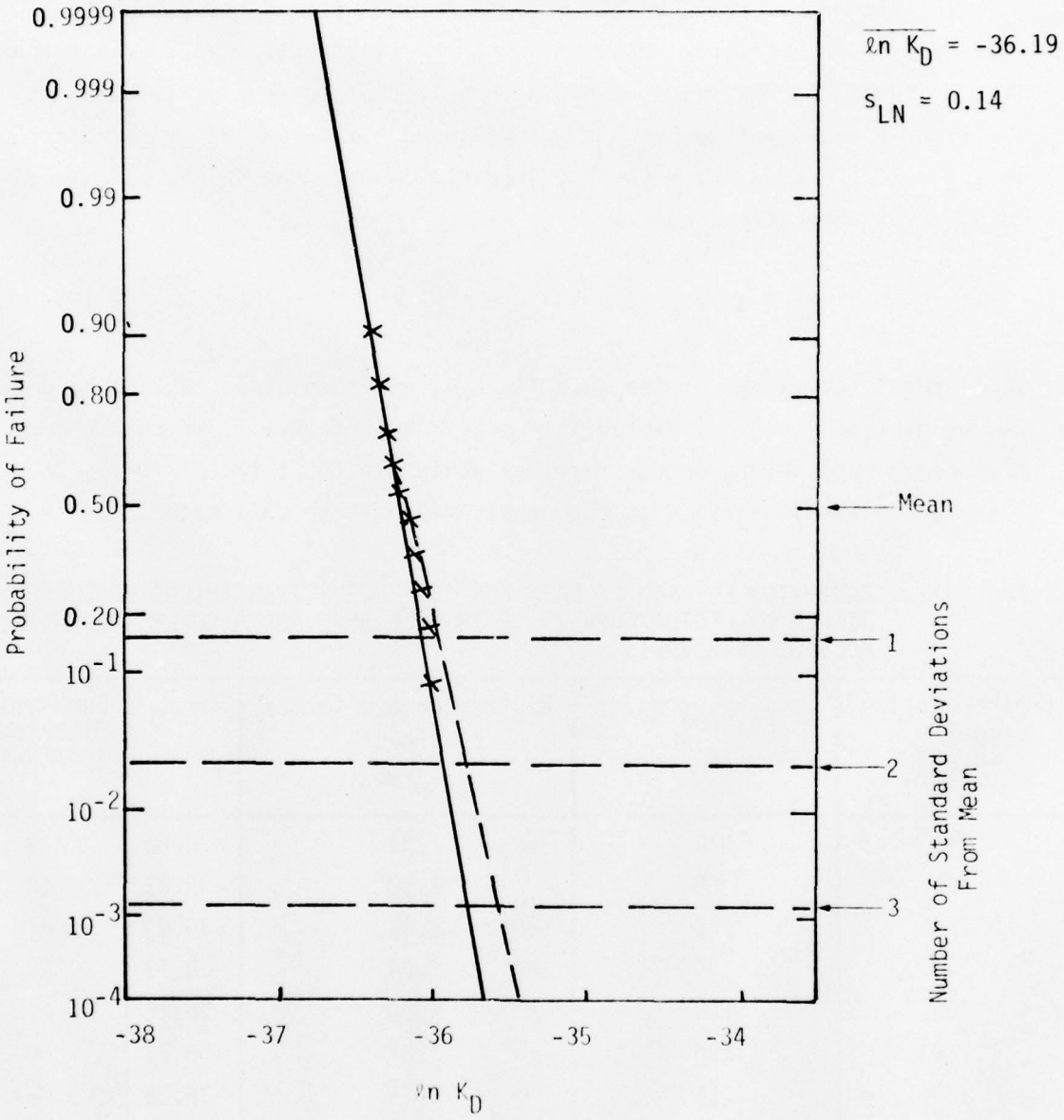

Figure 2. Cumulative frequency distribution of the natural logarithm of the neutron damage factor (K_D) for 10 samples from one lot of 2N2222 transistors. The line labeled P is the estimate of the upper bound of ℓn K_D for the population at 90 percent confidence.

Since the data from figure 2 are from a finite sample size, it is necessary to establish an estimate of upper bound of $\ell n\ K_D$ for the population at some level of confidence. This is done using

$$\overline{\ell n\ K_D} + K_{TL} s_{LN} \qquad (6)$$

where s_{LN} is the standard deviation of the lognormal data calculated from

$$s_{LN} = \left[\frac{\sum_{i=1}^{N} (\ell n\ K_{Di} - \overline{\ell n\ K_D})^2}{N - 1} \right]^{1/2} . \qquad (7)$$

$\overline{\ell n\ K_D}$ is the mean of the lognormal data and K_{TL} is the one-sided tolerance limit factor for a normal distribution.[13] K_{TL} values for different sample sizes and probabilities of failure at 90 percent confidence are given in figure 3. Using K_{TL} values from figure 3 and substituting into equation 6 establishes the line labeled P in figure 2. This line is the estimate of the upper bound of the population $\ell n\ K_D$ values. From figure 2 it can be seen that 99.99 percent of the 2N2222's from this population will have K_D values less than $e^{-35.43}$ or 4.08×10^{-16} (at 90 percent confidence).

It is not necessary to plot $\ell n\ K_D$ since $\overline{\ell n\ K_D}$ and s_{LN} are easily calculated on most pocket calculators. The advantage of plotting is to check the shape of the distribution (condition b).

4. APPLICATION OF HARDNESS ASSURANCE

Section 2 listed HA requirements. Section 3 provided the basic tools for HA. In this section, the results of the two previous sections are used to establish the category II criteria (determine whether HA is necessary) and to show the accept/reject procedure for category I parts.

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[13] A. Duncan, Quality Control and Industrial Statistics, R. D. Irwin, Inc., Homewood, IL, 1959.

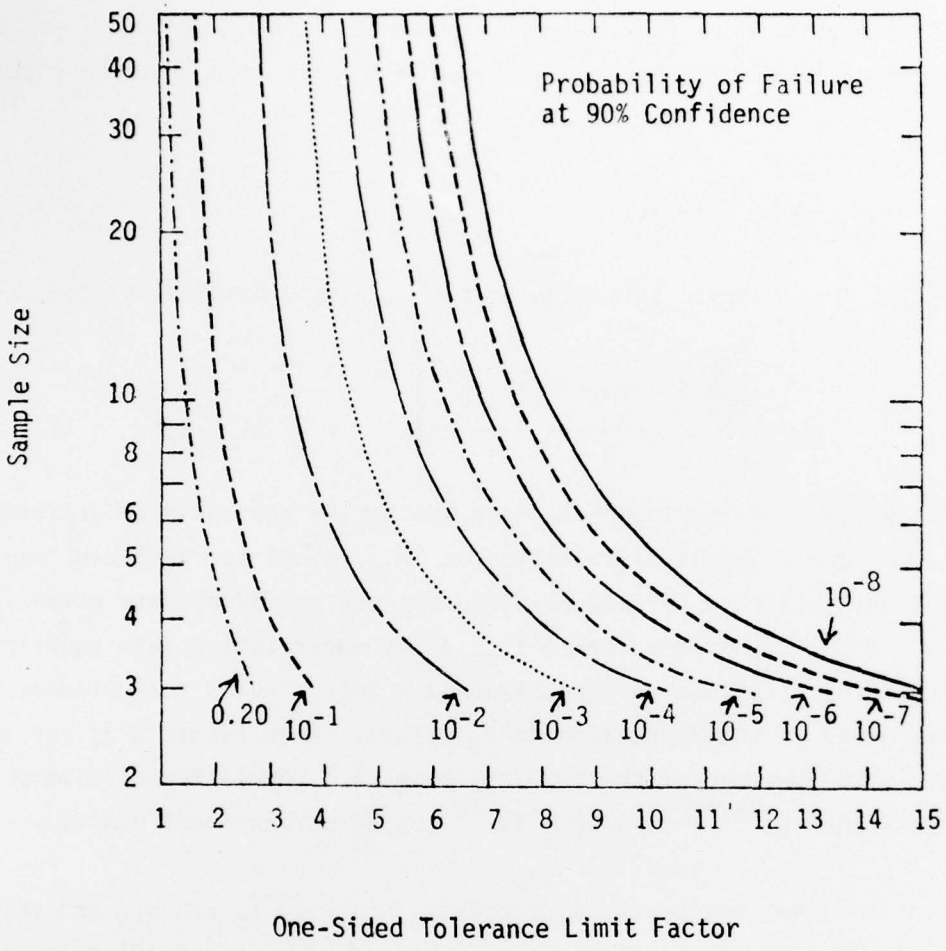

Figure 3. One-sided tolerance limit factor for normal distribution as function of failure probability at 90 percent confidence.

4.1 Transistor Neutron Design Margin Calculation

In section 2.2 the NDM was defined as the ratio of Φ_{MF} to Φ_{SPEC}. If the piece-part is known to have a parameter whose change is proportional to fluence, this definition can be extended. For example, equation 1 shows that bipolar transistor reciprocal common emitter current gain changes proportionally with fluence. By defining K_{SPEC} in terms of Φ_{SPEC},

$$K_{SPEC} = \frac{2\pi f_T}{\Phi_{SPEC}} \left[1/h_{FE(FAIL)} - 1/h_{FEO}\right]$$

and K in terms of Φ_{MF}

$$K = \frac{2\pi f_T}{\Phi_{MF}} \left[1/h_{FE(FAIL)} - 1/h_{FEO}\right]$$

the NDM for bipolar transistors can be expressed as

$$NDM = \frac{K_{SPEC}}{K} . \qquad (8)$$

This definition of the NDM is independent of an assumed population distribution. However, system HA interpretation depends on the assumption of a distribution by which one can extrapolate small sample data to the low P_F values needed for practical systems applications. For example, by assuming a lognormal distribution, measuring the mean ($\overline{\ell nK}$) and variance (s_{LN}) of a sample of size N, and selecting K_{TL} at a specified P_F, it can be shown that P_F will not be greater than its specified value if

$$NDM \geq e^{K_{TL} s_{LN}} .$$

This follows from the expression of the NDM in terms of K when applied to lognormal space

$$NDM = \frac{e^{\ell n\ K_{SPEC}}}{e^{\overline{\ell nK}}}$$

where

$$\ell n\ K_{SPEC} = \overline{\ell nK} + K_{TL} s_{LN}.$$

From the above discussion it can be seen that the NDM is a ratio of a measurable quantity (K) and a requirement (K_{SPEC}). It is used to account for piece-part variability and other uncertainties. If it can be asserted that the upper limit to the standard deviation of a lognormal generic piece-part population distribution is σ_{WC}, then

$$NDM = e^{K_\sigma\ \sigma_{WC}}$$

where K_σ is the number of standard deviations for which the residual area under the lognormal distribution is less than P_F.

Messenger has gathered data on K for 345 assorted bipolar transistors and analyzed it using f_T to normalize between different transistor types.[14] The distribution of the data was approximately lognormal with an s_{LN} of 0.42.[15] A value for σ_{WC} of 0.493 has been estimated by Namenson from this data.[16] Using this value for σ_{WC} and the equation above, table III gives values of the NDM for a specified P_F.

The design margin of 10 for neutron damage given by Patrick and Ferry can be translated into a P_F using table III.[3] As can be seen, an NDM of 10 corresponds to a P_F of about 2×10^{-6}.

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[3] R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines for Systems with Moderate Requirements, Air Force Weapons Laboratory, Kirtland AFB, NM, AFWL-TR-76-147, September 1976.

[14] G. Messenger and E. Steele, Statistical Modeling of Semiconductor Devices for the TREE Environment, IEEE Trans. Nucl. Sci., NS-15, 133, December 1968.

[15] D. Alexander, et al., Hardening Options for Neutron Effects - An Approach for Tactical Systems, Harry Diamond Laboratories, Adelphi, MD, HDL-CR-74-052-1, November 1976.

[16] A. Namenson, Statistical Treatment of Damage Factors for Semiconductor Devices, to be published.

TABLE III. TRANSISTOR NEUTRON DESIGN MARGINS (NDM'S) FOR MAXIMUM PROBABILITY OF FAILURE (P_F) AT 90 PERCENT CONFIDENCE.*

P_F	NDM	K_σ
1×10^{-1}	1.9	1.28
1×10^{-2}	3.1	2.3
1×10^{-3}	5.1	3.3
1×10^{-4}	6.8	3.9
1×10^{-5}	8.3	4.3
1×10^{-6}	11	4.8
1×10^{-7}	13	5.2
1×10^{-8}	15	5.5

* Calculated from the 345 unit sample data of Messenger: G. Messenger and E. Steele, Statistical Modelling of Semiconductor Devices for the TREE Environment, IEEE Trans. Nucl. Sci., NS-15, 133, December 1968, assuming a lognormal population worst-case standard deviation of 0.493.

The use of the NDM in the procedure of figure 1 can now be detailed. First, the desired P_F at 90 percent confidence is identified from the application requirements. The NDM corresponding to the P_F is then identified using Table III. The category II criterion is then given by equation 3:

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC}.$$

To illustrate the procedures developed to this point, refer to figure 1 and consider the following example. Suppose that it is required to use a 2N2222 in a circuit with an $h_{FE(FAIL)}$ specification of 40 at a collector current (I_C) of 10 mA, a collector voltage of 10 V, a Φ_{SPEC} of 2×10^{13} n/cm^2, and the P_F specification for the part is 1×10^{-4}.

Step 1. Determine whether Φ_{SPEC} is less than Φ_{TH}. Φ_{TH} for transistors was calculated in section 2.1 to be 1×10^{10} n/cm^2. Since Φ_{SPEC} is larger than Φ_{TH} proceed to step 2 (or level 2 in figure 1).

Step 2. Determine whether HA is necessary. The category II criterion is given by equation 3:

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC} .$$

The NDM at a P_F of 1×10^{-4} is found from table III to be 6.8. Φ_{MF} is found from equation 4:

$$\Phi_{MF} \geq \frac{2\pi f_{T(MIN)}}{K} \left[1/h_{FE(FAIL)} - 1/h_{FE(MIN)} \right] .$$

By substitution ($h_{FE(MIN)}$ is 75 and $f_{T(MIN)}$ is 250 MHz from the manufacturer's specification sheet),

$$\Phi_{MF} \geq \frac{2\pi(250)(10^6)}{(0.8)(10^{-6})} \left[1/40 - 1/75 \right]$$

or Φ_{MF} is 4.3×10^{12} n/cm^2. Now $\Phi_{MF}/6.8$ is not greater than Φ_{SPEC}, so HA is needed and the 2N2222 is category I. Category I procedures (level 3 in figure 1) are covered in the next section.

4.2 Category I Procedures

Category I parts are those parts which need HA controls, monitoring, and evaluation efforts. If part substitution cannot be used to obtain a larger design margin, then these efforts must be done to keep part variations within known and acceptable limits. The HA efforts for category I parts are implemented through procurement specifications, which were discussed in section 2.3.

The criterion for lot acceptance of category I parts is $\Phi_F > \Phi_{SPEC}$. For bipolar transistors, this is equivalent to $K_{DF} > K_{D(SPEC)}$, where K_{DF} is found from

$$K_{DF} = e^{\overline{\ell n K_D} + K_{TL} s_{LN}}$$

at the desired P_F.

While the NDM is not used by the parts procurement activity, it is useful as a quantification of the tradeoff between design procedures and procurement cost. If the sampled production population (date code, diffusion lot, etc.) distribution is much narrower than the entire population (if s_{LN} is much smaller than σ_{WC}) the NDM decreases even though the K_{TL} multiplier will be larger than K_σ due to finite sample size. The NDM is calculated using

$$NDM = e^{K_{TL} s_{LN}} .$$

The penalty of using a smaller NDM is the cost of lot-sample testing.

To illustrate the procedures for category I parts, let us continue the example started in section 4.1. Since step 2 in the example indicated that the 2N2222 was a category I part, proceed to level 3 in figure 1 (step 3 in the continuing example).

Step 3. If HA is necessary, procure an S-1 or S-2 device and perform accept/reject testing.

Since the purpose of neutron radiation lot-sample testing is to characterize the production population from which the sample was obtained, the population needs to be as homogeneous as possible and should therefore be from one date code (if possible from one diffusion lot). The procedure

is to draw a minimum sample of devices (5 to 20) from the lot, subject the sample to neutron radiation (around the level of interest or at the 20, 50, and 80 percent parameter degradation levels), and compute the mean and standard deviation. If the estimate of the upper bound of the population value meets circuit specifications, then devices from that lot can be accepted.

Suppose that one lot of 30 2N2222 devices was purchased from one manufacturer with one date code and that a sample of 10 devices from that lot gave the radiation data listed in table 2 and plotted in figure 2. These data had a $\overline{\ell n\ K_D}$ value of -36.19 and an s_{LN} of 0.14. The estimate of the upper bound of K_D for the lot is calculated using equation 6 and a K_{TL} value from figure 3 corresponding to the sample size and the desired P_F. For a sample size of 10 units and a P_F of 1×10^{-4}, K_{TL} is determined to be 5.4 from figure 3. Substitution into equation 6 yields a K_D of

$$e^{(-36.19)+(5.4)(0.14)} = 4.1 \times 10^{-16}\ cm^2/n\ .$$

We have now determined that 99.99 percent (one minus the P_F of 1×10^{-4}) of the 2N2222's in the purchased lot have K_D values below 4.1×10^{-16} cm^2/n. This value of K_D can be translated into Φ_F using equations 2 and 4

$$\Phi_F \geq \frac{1}{K_D}\left[1/h_{FE(FAIL)} - 1/h_{FE(MIN)}\right] \qquad (9)$$

$$\geq \frac{1}{(4.1)(10^{-16})}\left[1/40 - 1/75\right]$$

$$\geq 2.9 \times 10^{13}\ .$$

Since Φ_F for this lot is above Φ_{SPEC}, the lot can be accepted.

Suppose a sample of only three devices was taken from the 30 unit 2N2222 date code lot. Would the lot still be accepted? The value of K_{TL} in this case would be 10.4 (from figure 3) which would yield a K_D of 8.2×10^{16} cm^2/n and hence a Φ_F of 1.4×10^{13} n/cm^2 (instead of 2.9×10^{13} n/cm^2), which is too low to be accepted. This illustrates the need to choose a sample size of at least 5 (preferably 10) to reduce the sensitivity of K_{TL} to sample size (the curves of figure 3 have a steep slope for sample sizes of 10 or more).

4.3 Transistor Logic Circuits

To illustrate the procedure for transistors used in logic circuits or in switching applications, consider the following example. Suppose we wish to use the 2N2222 in the logic circuit of figure 4. The environmental and P_F specifications are 1×10^{13} n/cm^2 and 1×10^{-4} respectively.

The circuit of figure 4 has an I_C of 2 mA and an I_B of 0.2 mA which yields a forced h_{FE} (h_{FEF}) of 10. When h_{FE} (which is measured in the active region with $V_{CE} > 1V$) is degraded by neutrons to the h_{FEF} value, the transistor will come out of saturation. The ideal value for h_{FEF} will be that value that will allow sufficient penetration of the saturation region to allow V_{CE} to be a linear function of the I_C. A rule of thumb is given by[17]

$$h_{FEF} = \frac{h_{FE}}{1.3} \quad .$$

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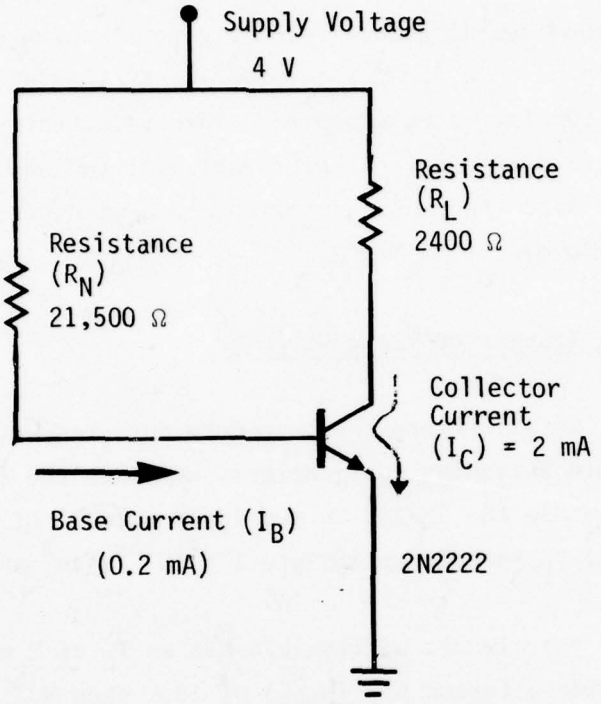
[17]Switching Transistor Handbook, Motorola Corporation, 1963.



$$I_C = \frac{V_{CC} - V_{CE}}{R_L} = \frac{5.0 - 0.25}{2400} = 2 \text{ mA}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_N} = \frac{5.0 - 0.7}{21,500} = 0.2 \text{ mA}$$

$$h_{FEF} = \frac{I_C}{I_B} = \frac{2 \text{ mA}}{0.2 \text{ mA}} = 10$$

Figure 4. Logic circuit example of forced beta (h_{FEF}) calculation.

A simple calculation illustrating the concept of h_{FEF} and h_{FE} is given in figure 4. The resistor values and the supply voltage determine I_C and I_B. The ratio of I_C to I_B is 10. If the selected transistor is a 2N2222, the manufacturer's data sheet lists $h_{FE(MIN)}$ measured in its active region at a current of 2 mA to be 60. Therefore, the minimum overdrive factor ($h_{FE(MIN)}/h_{FEF}$) for saturation is 6.0. Since the rule of thumb for saturation is an overdrive factor of 1.3 or more, the device is in saturation. It will come out of saturation if neutrons cause h_{FE} to be reduced from 60 to (10)(1.3) or 13. At that point, the device starts to go into its linear region, and the V_{CE} rises to a point where the circuit can no longer perform its required function. From this description it can be seen that h_{FEF} is a circuit concept and not a device concept.

To see if HA is necessary in this example, use the category II criterion given by equation 3

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC}$$

where Φ_{MF} is given by equation 4

$$\Phi_{MF} \geq \frac{2\pi f_{T(MIN)}}{K}\left[1/h_{FE(FAIL)} - 1/h_{FE(MIN)}\right]$$

$$\geq \frac{2\pi(250)(10^{6})}{(0.8)(10^{-6})}\left[1/13 - 1/60\right]$$

$$\geq 1.2 \times 10^{14}.$$

At a P_F of 1×10^{-4}, table III gives an NDM of 6.8, which yields a Φ_{MF}/NDM value of 1.8×10^{13}. Since this value is greater than Φ_{SPEC}, HA is not needed.

5. HARDNESS ASSURANCE MANAGEMENT

HA management activities are described only briefly in this section. This subject is discussed in detail by Patrick and Ferry.[3]

5.1 Procurement Procedures

Those piece-parts that can meet the NDM requirement for no HA controls (according to the procedures of section 4) are identified in a parts list as category II parts. They are procured according to high reliability non-nuclear specifications. Those piece-parts that cannot meet the NDM requirement and therefore require HA should be procured according to HA procurement specifications. They are identified in a parts list as category I parts so that the radiation-critical items of a system can be easily and rapidly identified.

Category I parts should be from one date code. In cases where very narrow distributions are required, a single diffusion lot may be needed. Most category I parts need S-1 control procedures that require radiation lot-sample testing. Accept/reject decisions are made based on lot-sample statistics and circuit requirements according to the procedure of section 4.

5.2 Documentation

HA monitoring efforts (screens and radiation test data) should be documented to build a data base that will build confidence in HA procedures. The subject of documentation is covered by Patrick and Ferry.[3]

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[3] R. Patrick and J. Ferry, Nuclear Hardness Assurance Guidelines for Systems with Moderate Requirements, Air Force Weapons Laboratory, Kirtland AFB, NM, AFWL-TR-76-147, September 1976.

5.3 Cost Impact of Hardness Assurance

The impact and the benefits of HA for S-2 and S-1 controls need to be examined so that a benefit-to-cost ratio can be determined. No attempt is made here to develop a detailed cost model; that is beyond the scope of this document. Also, prices vary widely due to market forces; so a detailed production cost model is irrelevant. For example, a sole-source request for an f_T screen would probably cost more than a MIL-SPEC f_T screen requirement.

To reduce the importance of market forces and to identify cost adders, assume a 1000-unit procurement quantity of 2N2222 transistors on a non-sole-source basis. The 2N2222 S-1 level cost adders are

a. C_B, basic part cost

b. C_{JAN}, military requirement

c. C_{TRAC}, diffusion lot traceability

d. C_S, electrical screens

e. C_{RAD}, lot-sample radiation.

Since C_B and C_{JAN} costs are beyond the scope of this document, assume that C_{JAN} is three times the C_B cost. The C_{TRAC} support costs depend on volume and run about \$2000 for 1000 units. Since these costs can be spread over the purchase quantity, C_{TRAC}/N is used in the cost formula to be developed. The C_{RAD} costs are based on reactor time (~\$250/hour in 1979 dollars) plus the time required for preirradiation and postirradiation measurements. A sample of 30 2N2222's would be sufficient to characterize the 1000 purchase quantity and would cost about \$600. The C_{RAD} costs, like the C_{TRAC} costs, depend on volume and can therefore be spread over the purchase quantity.

The cost formula (C_T) for a 2N2222 can now be given:

$$C_T = C_B + C_{JAN} + \frac{C_{TRAC}}{N} + \frac{C_S}{Y} + \frac{C_{RAD}}{NY}$$

where Y is the yield. Since rejected devices are not thrown away, Y can be 100 percent. In terms of the basic unit cost, a rough calculation shows that an S-2 control part ($C_{TRAC} + C_S$) can cost about 12 times more than a basic part. An S-1 control part ($C_{TRAC} + C_S + C_{RAD}$) can cost about 15 times more than a basic part.

The cost factors for HA control levels 1 and 2 in terms of basic and JAN class A costs are given below.

Basic	JAN	Captive Strategic Line	Control Level 2	Control Level 1
1	X3	X13	X12	X15
-	1	7	X5	X7

These approximate cost factors apply only to small scale-integrated devices. Note that the cost of a part goes up by about a factor of 10 if HA controls are implemented.

6. SUMMARY

HA includes all control, monitoring, and evaluation efforts aimed at procuring systems whose nuclear hardness equals or exceeds that of the design-hardened engineering prototype. The guideline procedures developed in this document are illustrated in figure 1. The procedure is based on a successive elimination of piece-parts with acceptable probabilities of survival.

The first level in figure 1 asks if Φ_{SPEC} is above Φ_{TH}. Φ_{TH} values for the different generic device families are as follows:

a. Transistors. Φ_{TH} for transistors was calculated in section 2.1 from a worst-case theoretical model to be 1×10^{10} n/cm^2.

b. Reference diodes. The most sensitive reference diodes are the temperature-compensated types. Φ_{TH} for temperature-compensated reference diodes is determined in appendix B to be 4×10^{10} n/cm^2.

c. TTL digital integrated circuits. Φ_{TH} for TTL circuits is given in appendix C as 1×10^{10} n/cm^2.

d. Operational amplifiers. Φ_{TH} for operational amplifiers and transistors is the same (1×10^{10} n/cm^2) for the reasons discussed in appendix D.

e. JFET's. Φ_{TH} for JFET's is calculated in appendix E from an estimate of the carrier removal rate and the worst-case channel doping to be 2×10^{13} n/cm^2.

The second level in figure 1 asks if HA is needed. This question is answered in one of two ways: (1) by calculating worst-case degradation from a model using manufacturer-specified data or (2) by determining if the NDM is adequate.

The NDM criterion for category II devices (no HA needed) was given in section 2.2, equation 4, as

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC} \quad .$$

The NDM is selected at an application-specified P_F from a statistical analysis of data which represents lot-to-lot and manufacturer-to-manufacturer variations. Values for Φ_{MF} and the NDM for the generic families covered in this document are as follows:

a. Transistors. For transistors, the required NDM is obtained at the application-specified probability of failure at 90 percent confidence from table III. Φ_{MF} is given in section 2, equation 4, as

$$\Phi_{MF} \geq \frac{2\pi f_{T(MIN)}}{K} \left[1/h_{FE(FAIL)} - 1/h_{FE(MIN)} \right]$$

where K is 0.8×10^{-6} $cm^2/n \cdot s$ for transistors operated near the maximum I_C point for h_{FE}. If I_C is one-tenth that of the maximum h_{FE} point, K should be increased to 2×10^{-6}; if it is one-hundredth that of the maximum h_{FE} point, K should be increased to 7×10^{-6} $cm^2/n \cdot s$.

b. Reference diodes. An NDM has not been established for reference diodes.

c. TTL digital integrated circuits. Since the variation in TTL units is expected to be much less than that of discrete transistors, the NDM for transistors (table III) can be used as a conservative value. Φ_{MF} is developed in appendix C to be

$$\Phi_{MF} \geq \left[\frac{2\pi f_{T(MIN)}}{(0.8)(10^{-6})} \right] \left[I_{B(MIN)} \left(1/I_{SK(FAIL)} - 1/I_{SK(MIN)} \right) \right]$$

where $I_{B(MIN)}$ is the minimum base current to the output transistor calculated from circuit analysis, I_{SK} is the sink current, and $f_{T(MIN)}$ is 250×10^6 Hz if no better estimate is available.

d. Operational amplifiers. The NDM for transistors (table III) is used together with

$$\Phi_{MF} \geq \frac{4\pi f_{T(MIN)}}{(7 \times 10^{-6}) I_{E(MAX)}} \left[I_{B(FAIL)} - I_{B(MAX)} \right]$$

to establish the category II criterion. If no better estimates are available use 250×10^6 Hz for $f_{T(MIN)}$, 10×10^{-6} for the LM108A $I_{E(MAX)}$, 40×10^{-6} for the LM101A $I_{E(MAX)}$, and 20×10^{-6} for the 741 $I_{E(MAX)}$. These estimates together with a $2I_{B(MAX)}$ failure criterion give a Φ_F of 3×10^{11}, 1×10^{12},

and 1×10^{13} for the LM108A, LM101A, and 741, respectively. The category II breakpoint at a P_F of 10^{-4} (an NDM of 6.8 obtained from table III) is thus an Φ_{SPEC} of 5×10^{10} for the LM108A, 1×10^{11} for the LM101A, and 1×10^{12} for the 741 based on these rough estimates.

e. JFET's. An NDM has not been established for JFET's, as explained in appendix E.

If HA is needed, then the third level in figure 1 is reached. Category I parts (those parts needing HA) are procured at one of two control levels (S-1 or S-2) as detailed in the procurement specification. Level S-2 requires electrical screens and process controls. Level S-1 requires all the controls and monitoring efforts of level S-2 plus radiation lot quality conformance tests.

The procedure for radiation lot quality conformance testing is to draw a random sample of devices (5 to 20) from one date code and subject the sample to radiation around the level of interest as defined by the application, or at the 20, 50, and 80 percent degradation levels. The purpose of the radiation tests is to establish a Φ_F for each part using the application-defined values for bias, operating levels, and failure definition. The Φ_F data are then converted to natural logarithms, and the mean ($\ell n\ \Phi_F$) and standard deviation (s_{LN}) are calculated from the statistical formulas of section 3.2. The Φ_F level for the lot is then established from

$$\Phi_F = e^{(\ell n\ \Phi_F + K_{TL} s_{LN})}$$

where K_{TL} is the one-sided tolerance limit factor selected from figure 3 based on the size of the sample and the specified probability of failure. If Φ_F is greater than Φ_{SPEC}, then the lot can be accepted.

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14. G. Messenger and E. Steele, Statistical Modeling of Semiconductor Devices for the TREE Environment, IEEE Trans. on Nucl. Sci., NS-15, 133, December 1968.

15. D. Alexander et al., Hardening Options for Neutron Effects - An Approach for Tactical Systems, Harry Diamond Laboratories, Adelphi, MD, HDL-CR-74-052-1, November 1976.

16. A. Namenson, Statistical Treatment of Damage Factors in Semiconductor Devices, to be published.

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GLOSSARY, SYMBOLS, AND ABBREVIATIONS USED

Category I	Piece-parts identified as category I require HA procedures.
Category II	Piece-parts identified as category II do not require HA procedures.
f_T	Transistor common emitter gain-bandwidth product expressed in s^{-1}.
h_{FE}	Common emitter current gain.
h_{FEO}	Common emitter current gain before radiation.
$h_{FE(RAD)}$	Common emitter current gain after radiation.
$h_{FE(MIN)}$	Minimum common emitter current gain specified by the manufacturer for the piece-part before radiation.
$h_{FE(FAIL)}$	The specified common emitter current gain at which circuit failure will occur.
h_{FEF}	The circuit forced h_{FE} which is determined by the ratio of the collector current to the base current.
HA	Hardness assurance (HA) includes all control, monitoring, and evaluation efforts aimed at procuring systems whose nuclear hardness equals or exceeds that of the design-hardened engineering prototype.
I_B	Transistor DC base current.
I_C	Transistor DC collector current.
K	Average lifetime damage constant expressed in $cm^2/n \cdot s$.
K_D	Neutron damage factor expressed in cm^2/n.
K_{DF}	The application-defined failure damage factor at a given probability of failure.

K_{SPEC} — The application defined lifetime damage constant at some probability of failure.

K_{TL} — The one-sided tolerance limit factor for a normal distribution.

K_{σ} — Number of standard deviations for which the residual area under the lognormal distribution is less than some specified probability of failure.

$\overline{\ell n K_D}$ — The mean of the lognormal K_D data calculated from

$$\frac{\sum_{i=1}^{N} \ell n\ K_{Di}}{N}$$

NDM — The factor that relates the piece-part mean neutron failure fluence to the specified neutron fluence. Its value is calculated statistically from a population of devices representing lot-to-lot and manufacturer-to-manufacturer variations.

P_F — Probability of failure.

S-1 — Control level S-1 HA applies to category I devices and requires all of the S-2 controls plus radiation lot-sample tests.

S-2 — Control level S-2 HA applies to category I devices and requires process controls plus 100 percent non-degrading screens

s_{LN} — The standard deviation of the lognormal data calculated from

$$\sum_{i=1}^{N}\left[\frac{\left(\ell n\ K_D - \overline{\ell n\ K_D}\right)^2}{N - 1}\right]^{1/2} .$$

Φ — 1 MeV equivalent neutron fluence expressed in n/cm^2.

Φ_F — The piece-part application-defined failure neutron 1 MeV equivalent fluence expressed in n/cm^2 at a given probability of failure.

Φ_{MF} — The mean piece-part failure fluence.

Φ_{SPEC}	Circuit specified neutron 1 MeV equivalent fluence expressed in n/cm^2.
Φ_{TH}	The generic part neutron 1 MeV equivalent threshold fluence in n/cm^2 .
σ_{WC}	The upper standard deviation limit of a lognormal population.

APPENDIX A
TRANSISTOR WORST-CASE MODEL

A transistor model for displacement damage can be used to calculate worst-case damage constants (K_D's) for transistors. This approach offers two advantages over the statistical approach: (1) the nature of the distribution does not need to be assumed to get low failure probabilities and (2) the sensitivity of proposed HA controls can be evaluated.

The model assumes an ideal step-junction, uniform-base device.[1] This represents a worst case because a graded-base device with the same edge doping has an overall higher injection ratio, especially near the collector-base junction, and therefore a lower K_D. The value of h_{FE} in the model is determined by three components of base current: bulk-base recombination, emitter-base depletion layer recombination current, and base-emitter minority carrier reverse diffusion into the emitter. The base-emitter surface leakage current and collector-base reverse-bias leakage current are neglected.

The model input consists of six physical parameters: emitter lifetime (approximately 1×10^{-8} s if not known), emitter doping (approximately 3×10^{18} atoms/cm^3 if no better estimate can be found), base width, maximum base doping, minimum base doping, and emitter area. The last four physical parameters are calculated from the following electrical parameters: minimum f_T, emitter-base breakdown voltage, collector-base breakdown voltage, and maximum input capacitance.

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[1] A. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, IEEE Trans. Nucl. Sci., NS-24, 2093, December 1977.

The model calculates the upper bound value of K_D using

$$K_D \approx \frac{W_b^2 K_b}{0.052\mu_b(1 + Z)[1 + (C - 1)Z]}$$

$$+ \frac{6.2\mu_e^{\frac{1}{2}} N_B W_b \left[\left(\frac{1}{\tau_e} + K_e\Phi\right)^{\frac{1}{2}} - \left(\frac{1}{\tau_e}\right)^{\frac{1}{2}}\right]}{\mu_b N_E (1 - Z^2)\Phi}$$

$$+ \frac{(2.5)(10^7)\left(\frac{W_b^5 I_C^2}{\mu_b A_e^2}\right)^{1/3} \left\{\ell n\left[\frac{(4.2)(10^{-21}) N_E A_e \mu_b}{W_b I_C}\right]\right\}^{\frac{1}{2}} (1 - Z)}{N_B^{5/6} \ell n\left[\frac{N_E N_B}{(2.3)(10^{20})}\right] Z(1 + Z)}$$

where W_b = vertical distance between emitter and collector regions (base width under emitter well) in centimeters,

K_b = lifetime damage constant for base region in square centimeters per neutron second,

μ_b = mobility in base region in square centimeters per volt second,

N_B = base doping concentration in atoms per cubic centimeter,

K_e = lifetime damage constant for emitter region in square centimeters per neutron second,

N_E = emitter doping concentration in atoms per cubic centimeter,

A_e = projected emitter area in square centimeters,

Z = minority carrier injection ratio,

I_C = collector current in Amperes,

Φ = neutron fluence in neutrons per square centimeter,

τ_e = emitter minority carrier lifetime in seconds,

C = ratio of high injection minority carrier lifetime to low level lifetime.

The dependence of K_D on I_C as calculated from the model is in excellent agreement with experimental results up to the I_C value corresponding to peak h_{FE}. Beyond this level, current crouwding becomes important. Current crowding in an epitaxial bipolar transistor occurs when the base current flows from the base contact to the base region under the emitter, producing a voltage gradient over this base region. The internal base voltage produces a net junction potential that decreases from the periphery to the center of the emitter. The higher edge forward potential crowds the injected emitter current into the peripheral areas of the emitter well, which effectively reduces the active cross-sectional area. The internal base bias may be such that the injected carrier density in the center of the emitter junction may actually be zero. Any resultant increase in the base current produced by neutron bombardment further aggravates this current-crowding effect and thus complicates the analysis of gain degradation.

A computer solution to the above equation for K_D has been written in BASIC and makes the solution fast and simple.[2] For the 2N2222, the model yields $K_D = 6 \times 10^{-15}$. This is roughly equivalent to the K_D value obtained from the 2N2222 statistical data of section 4 using a $f_{T(MIN)}$ of 250 MHz, divided by the NDM at a P_F of 1×10^{-6}. From section 4

$$K_D = \frac{K}{2\pi f_{T(MIN)}}$$

$$= \frac{(0.8)(10^{-6})}{2\pi(250)(10^6)}$$

$$= 6 \times 10^{-16}$$

and the NDM at a P_F of 1×10^{-6} is 11. The statistical upper bound value of K_D is thus 5×10^{-15} cm^2/n, which is close to the 6×10^{-15} value obtained above from the model.

[2] A. Hart et al., Parameter Sensitivities for Hardness Assurance: Displacement Effects in Bipolar Transistors, Mission Research Corporation, La Jolla, CA; MRC/SD-R-20, December 1977.

APPENDIX B
REFERENCE DIODE HARDNESS ASSURANCE

B-1. EFFECTS OF NEUTRON RADIATION

Voltage reference diodes are PN junction devices operated in the reverse direction with sufficient bias to cause avalanche or Zener breakdown. The desired property of the voltage reference diode is that very little current flows until the specified breakdown voltage. At breakdown, the Zener or avalanche processes should allow large current flows so that the voltage drop across the diode remains essentially constant over many decades of current. This kind of diode can be used as a voltage reference element since the voltage across it is independent of the current through it as long as the voltage remains above the breakdown voltage of the diode. For avalanche breakdown diodes, the breakdown voltage is a function of the impurity doping levels (and other parameters) and increases with neutron radiation. Zener diodes above 7 to 8 V exhibit avalanche breakdown.

Zener breakdown is similar to avalanche breakdown except that the breakdown results from band-to-band tunneling. In this mechanism, carriers tunnel from the conduction band of the heavily doped N region across the forbidden gap to the valence band of the heavily doped P region. Diodes operating in Zener breakdown exhibit relatively low breakdown voltages (less than about 6 V), with a breakdown characteristic somewhat softer than those diodes that are avalanching. Voltage reference diodes based on Zener breakdown show a decrease in the breakdown voltage with neutron fluence.

The high doping levels found in diodes make them inherently radiation resistant. Typically, for a silicon reference diode, a one percent change in the breakdown voltage is not reached until neutron fluences exceed 1×10^{14} n/cm^2. [1]

While diodes are relatively radiation resistant, temperature compensated reference (TCR) diodes are not. [2] To achieve temperature compensation, diodes are used in series, one or more forward-biased and one reverse-biased. They are used this way so that the forward-biased PN junction, which has a negative temperature coefficient, can be used to compensate for the positive temperature coefficient of the reverse bias junction. Since forward-biased diodes are more neutron sensitive than reverse-biased diodes, the category II criterion discussion in the next section will be devoted to forward-biased diodes.

B-2. CATEGORY II CRITERION

Since the TCR diode is the diode of interest for moderate neutron environments, this section is limited to the category II criterion for the most neutron sensitive element in a TRC unit, the forward-biased diode. The forward voltage in a diode with a heavily doped P region is given by

$$V = 2 \frac{kT}{q} \ell n \frac{I_D \sqrt{\tau_n}}{qN_A A \sqrt{D_n}} \qquad \text{(B1)}$$

where τ_n is the minority carrier lifetime in P-type material,

A is the junction cross-sectional area,

q is the electronic charge,

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[1] R.P. Donovan et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory, Dayton, OH, AFAL-TR-74-61, June 1974.

[2] D. Millward, Neutron HA Considerations for Temperature Compensated Reference Diodes, IEEE Trans. Nucl. Sci., NS-25, December 1978.

[3] TREE (Transient-Radiation Effects on Electronics) Handbook, Defense Atomic Support Agency, Washington, D.C., DASA 1420, September 1969.

D_n is the diffusion constant for electrons in P-type material,

N_A is the net acceptor concentration, and

I_D is the forward current.

The effect of neutron radiation is given by

$$\frac{1}{\tau_\Phi} = \frac{1}{\tau_o} + K_\tau \Phi \tag{B2}$$

where τ_Φ is the minority carrier lifetime at exposure Φ,

τ_o is the initial minority carrier lifetime,

K_τ is the lifetime damage constant, and

Φ is the total fast neutron fluence.

Differentiating equation B1 with respect to Φ yields

$$\frac{dV}{d\Phi} = \frac{kT}{q} \frac{1}{\tau_n} \frac{d\tau_n}{d\Phi} \quad . \tag{B3}$$

Differentiating equation B2 yields

$$\frac{d\tau_\Phi}{d\Phi} = \tau_\Phi^2 K_\tau \quad . \tag{B4}$$

Substitution of equation B4 into equation B3 and letting $\tau_\Phi = \tau_n$ yields the approximation

$$\Delta V \sim \left(\frac{kT}{q} K_\tau\right) \tau_n \Phi \quad . \tag{B5}$$

At room temperature, kT/q is 0.026 V, K_τ is 10^{-6} (from section 2.1), and a worst-case low doping level of 10^{15} cm^{-3} gives a τ_n of 10^{-6} s, which reduces equation B5 to a minimum estimate of the failure fluence Φ_F or

$$\Phi_F \geq (4 \times 10^{13})(\Delta V) \quad . \tag{B6}$$

Equation B6 can be used to calculate Φ_{TH}. Assuming that a 1 millivolt change in V is insignificant, equation B6 yields a value of 4×10^{10} n/cm for Φ_{TH}.

Attempts to establish a reasonable NDM for TCR diodes have not been successful due to the wide variations encountered from manufacturer to manufacturer (recent failure fluence data on a 1N829 TCR 6.2 V diode showed a change in $\overline{\ell n\ \Phi_F}$ of about a factor of 2).[2] Thus, the category II criterion for TCR diodes has not been established.

B-3. PROCUREMENT SPECIFICATIONS FOR HARDNESS ASSURANCE

For moderate neutron environments ($\Phi < 10^{13}$ n/cm^2), the minority carrier lifetime of the forward-biased diode is the dominant parameter that determines the neutron response of the TCR diode. Thus, lifetime and the number of forward diodes used for temperature compensation should be controlled.

An electrical screen on τ would be effective if it could be obtained from switching time measurements. Unfortunately, the back-to-back structure of the TCR diode makes switching time measurements somewhat ambiguous.

Because of wide variations in the neutron response of TCR diodes, the lack of an effective NDM, and the lack of adequate electrical screens, radiation sample testing (control level 1) by production lot or diffusion lot will be necessary for any neutron environment exceeding the Φ_{TH} calculated previously (4×10^{10} n/cm^2).

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[2] D. Millward, Neutron HA Considerations for Temperature Compensated Reference Diodes, IEEE Trans. Nucl. Sci., NS-25, December 1978.

An example procurement specification is given in Table B-1.

TABLE B-1. EXAMPLE PROCUREMENT SPECIFICATION FOR TEMPERATURE-COMPENSATED REFERENCE DIODES.

Hardness assurance control	Parameter	Test method	Test condition	Control level failure criterion S-2 Min	S-2 Max	S-1 Min	S-1 Max	Units
Process control	Resistivity profile	TBD[a]	TBD	-	TBD	-	TBD	-
	Doping material	TBD	TBD	-	-	-	-	-
Screen	None	-	-	-	-	-	-	-
Radiation quality conformance test	Φ	MIL-STD-883B-1017	I_{ZT} = TBD[b] $\Delta V_{Z(max)}$ = TBD	-	-	-	TBD	n/cm^2

[a] TBD means to be determined.

[b] Diode Zener current (I_{ZT}, the change in diode voltage (ΔV_Z), and the failure fluence (Φ_F) at a given probability of failure criteria is set by the circuit application.

B-4. HARDNESS ASSURANCE PROCUREMENT EXAMPLE

Suppose the circuit has the following specifications:

a. the specified fluence (Φ_{SPEC}) is 1×10^{12},

b. the reference current is 7.5 mA,

c. the maximum change in reference voltage is 5 mV,

d. the P_F is 1×10^{-4} at 90 percent confidence,

and a 1N829 TCR diode is required. The procedure is given in figure 1 as follows:

Step 1. Determine if $\Phi_{TH} \geq \Phi_{SPEC}$. Φ_{TH} is 4×10^{10} n/cm^2. Since Φ_{SPEC} is 1×10^{12}, proceed to step 2.

Step 2. Determine if HA is necessary. Since there is no NDM for TCR diodes, HA will be necessary.

Step 3. If HA is necessary, procure an S-1 control part and perform accept/reject testing. In this case, statistics are gathered on fluence using a maximum change in reference voltage as the failure criterion. Since the change in reference voltage (ΔV) is not linear with Φ (see equation B5), this problem cannot be handled like the transistor gain problem, which was covered in the body of the report. Instead, we are forced into a case 2A problem, which is discussed in appendix F. Case 2A calls for gathering statistics on Φ at a given ΔV failure criteria defined by the application.

Suppose a lot is procured from a manufacturer with a 14 unit sample lognormal mean failure fluence of 29.18 and a standard deviation of 0.19. Φ_F for the lot for a P_F of 1×10^{-4} at 90 percent confidence using a K_{TL} of 5 obtained from figure 3 is

$$\Phi_F = e^{29.18 - (0.19)(5)}$$

$$= 1.8 \times 10^{12} \text{ n/cm}^2$$

which is above the Φ_{SPEC} value of 1×10^{12}, so the lot can be accepted.

APPENDIX C
TRANSISTOR-TRANSISTOR LOGIC HARDNESS ASSURANCE

C-1. EFFECTS OF NEUTRON RADIATION

Transistor-transistor logic (TTL) is the most popular form of bipolar integrated circuit digital logic. In the 5400/7400 series, TTL devices come in five different versions at the present time: (1) the standard version (54/74), (2) the low-power version(L), (3) the high-speed version (H), (4) the Schottky version (S), and (5) the low-power Schottky version (LS). Figure C-1 shows the input and output differences between the families. [1]

The LS series (introduced in 1971), uses Schottky clamping of all saturating transistors to reduce storage times. Active pulldown of the base of the output transistor was added to square the transfer characteristics (figure C-1c). Also, the output pullup circuit uses a two-transistor Darlington connection to allow the output to pullup to one base-emitter voltage (V_{BE}) below collector voltage (V_C) for low values of output current. These LS-family features were incorporated to increase speed (6 ns average gate propagation delay) and reduce power consumption (2 mW average power per gate).

A typical TTL logic gate (the SN5400 gate, figure C-2) operates from a single 5 V power supply and has logic levels of 0.2 V for the binary 0 (low) and 3.4 V for binary 1 (high). This circuit consists of a

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[1] The TTL Data Book, 2nd edition, Texas Instruments, Inc., Dallas TX, 1976.

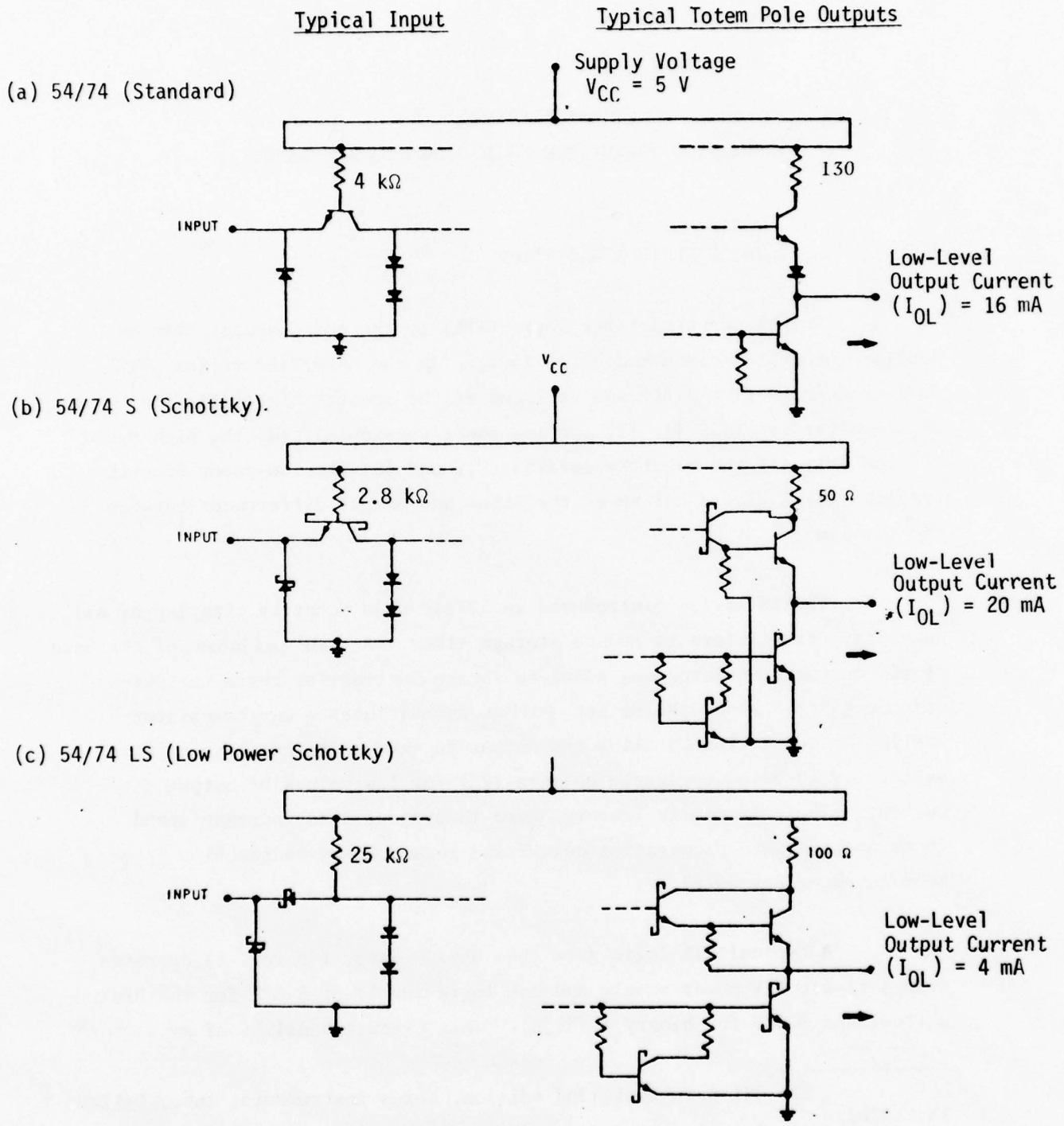

Figure C-1. Input-output comparison of SN54 and SN74 series transistor-transistor logic devices (from the TTL Data Book, 2nd edition, Texas Instruments, Inc., Dallas, TX 1976).

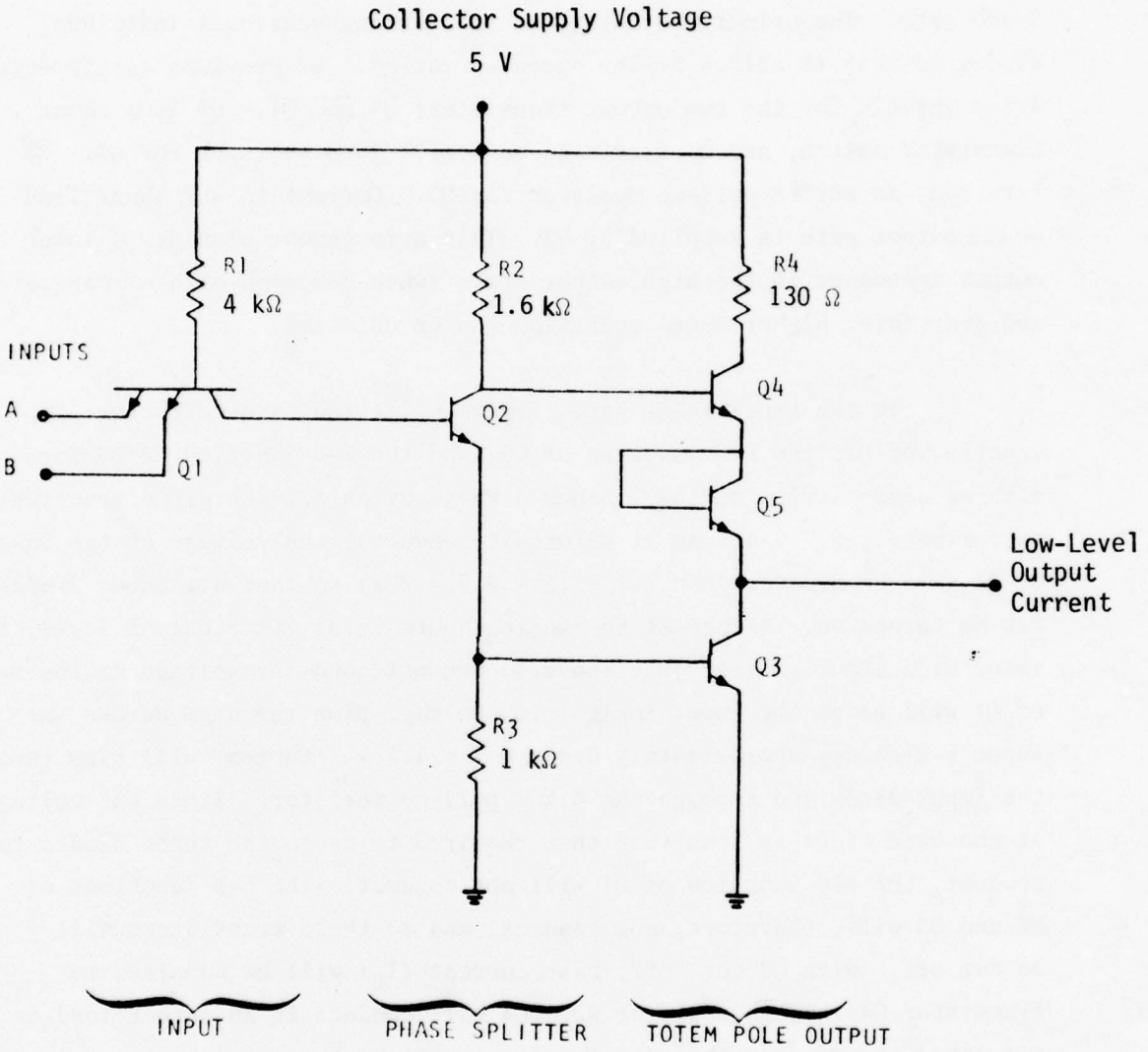

Figure C-2. Logic gate for SN5400 transistor-transistor logic device.

multiple emitter input transistor, Q1, a phase splitter transistor Q2, and a totem pole output circuit consisting of transistors Q3 and Q4. The multiple emitter-base (E-B) junctions of Q1, along with resistor R1, form a diode gate. The primary advantage of this arrangement over individual diodes is that it allows higher speed operation. Q2 provides complementary drive signals for the two output transistors Q3 and Q4. Q3 is a shunt transistor switch, and Q4 serves as an active load resistor for Q3. Q4 serves as an active pull-up resistor for Q3. Current to any shunt load on the output gate is supplied by Q4. This arrangement provides a lower output impedance in the high output state (when compared with a resistor), and therefore, higher speed operation can be obtained.

In the typical TTL gate (figure C-2), the base-collector (B-C) junction of Q1, the E-B junction of Q3, and the E-B junction of Q3 form a three-diode series string. Since a PN junction silicon diode requires approximately 0.7 V across it before it conducts, the voltage at the base of Q1 must be greater than 2.1 V ($3 \times 0.7 = 2.1$) so that all three diodes can be turned on. If one of the logic inputs is at its binary 0 level, the associated input emitter junction will conduct, and the voltage at the base of Q1 will be at the input logic level voltage plus the drop across the input E-B diode, approximately $0.4 + 0.7 = 1.1$ V. Current will flow through the input diode and through the 4 kΩ pull-up resistor. Since the voltage at the base of Q1 is less than that required to cause the three diodes to conduct, the B-C junction of Q1 will not conduct. The E-B junctions of Q2 and Q3 will, therefore, not conduct, and so these transistors will be cut off. With Q2 cut off, base current (I_B) will be supplied to transistor Q4 through resistor R2. Q4 will conduct if an output load is connected to ground. The output voltage will be the supply voltage less the drop across Q5, A4, and the 130 Ω collector resistor. Thus, a binary 0 voltage level at one or more of the inputs will produce a binary 1 output voltage level of between 2.4 and 3.6 V.

If a binary 1 logic level is applied to both inputs, the input will rise to 2.4 V or higher. With the E-B input diodes reverse-biased, the diode equivalent string will conduct through the 4 kΩ resistor since the voltage is above the required minimum of 2.1 V at the base of Q1. So the E-B junctions of Q2 and Q3 and the B-C junction of Q1 will be forward-biased. With Q2 conducting, its collector voltage will be lower than that required to turn Q4 on. Base current normally supplied to Q4 through Q2 will be shunted away by the conduction of Q2. With Q2 conducting, Q3 will saturate. At this time, the output voltage is the emitter-collector saturation voltage ($V_{CE(SAT)}$) of Q3, which will be about 0.4 V or less. Thus, with a binary 1 on both inputs, the output will be a binary 0.

In summary, TTL gates have a current sinking type of logic. They have a fan-out of 10, logic levels of +0.2 V for a binary 0 plus 3.3 V for a binary 1, a power dissipation of 2 mW, a propagation delay of 6 ns, and a supply voltage of 5 V (±10 percent).

C-2. CATEGORY II CRITERION

Satisfactory performance of TTL logic depends on the driving capability of the output transistor. As the gain of the output transistor (h_{FE}) decreases because of displacement damage, so does the output current of the TTL gate. The major effect is the reduction in the low-level output current (I_{OL}), which reduces the fan-out of the circuit. The primary parameter in determining I_{OL} is the h_{FE} of the output transistor. Although no simple analytical expression exists to relate I_{OL} to h_{FE} of the output transistor, it is approximately proportional to the h_{FE}.[2] Knowing the h_{FE} degradation characteristics of the output transistor therefore provides a reasonably good prediction of TTL gate performance, particularly under high fan-out conditions.

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[2] M. Simons, et al., Integrated Circuits for Radiation-Hardened Systems: A State-of-the-Art Review, Air Force Avionics Laboratory, Dayton, OH, AFAL-TR-76-194, January 1977.

The output sink current (I_{SK}) is related to the output transistor h_{FE} and can be measured by existing terminal parameters. I_{SK} is measured with the device in the low state by forcing sufficient current into the output of the device to drive the transistor out of saturation. I_{SK} is then limited by the h_{FE} of the output transistor. Since the I_B of the output transistor depends on resistors, V_{BE}, and $V_{CE(SAT)}$ of the internal transistors, it is essentially constant. This approach yields the neutron damage factor of the output transistor; however, it has several limitations that fortunately are of second-order importance: (1) circuit variations in V_{BE} and $V_{CE(SAT)}$ are not included, (2) resistor values depend on process variation, and (3) h_{FE} is measured at a fixed I_B. Since I_{SK} is made under conditions of constant I_B, collector current (I_C) can vary between units because of the variability of h_{FE}. Although this variation is not great, it can lead to difficulty because of the dependence of h_{FE} and the neutron fluence damage factor (K_D) on I_C. The variation of K_D and h_{FE} with I_C can be reduced by measuring I_{SK} at a lower collector supply voltage (V_{CC}).[3]

Using figure C-2 for the SN5400 gate, the output transistor gain h_{FE} is given by

$$h_{FE} = \frac{I_{SK}}{I_B} \qquad \text{(C1)}$$

where I_B is determined by circuit analysis to be

$$I_B \cong \frac{V_{CC} - 3V_{BE}}{R1} + \frac{V_{CC} - V_{CE(SAT)Q2} - V_{BE}}{R2} - \frac{V_{BE}}{R3} . \qquad \text{(C2)}$$

For the SN5400, one may assume that V_{CC} = 5V, V_{BE} = 0.7 V, and $V_{CE(SAT)Q2}$ = 0.2 V. Then I_B is approximately

$$I_B \cong \frac{5 - 3(0.7)}{(4)(10^3)} + \frac{5 - 0.2 - 0.7}{(1.6(10^3)} - \frac{0.7}{(1.0)(10^3)}$$

$$\cong 3 \text{ mA.}$$

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[3] Johnston and Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci., NS-21, 393, December 1974.

I_{SK} is measured with the input in the high state and with a voltage supply attached to the output and adjusted until the output voltage measured at the collector of Q3 is greater than $V_{CE(SAT)}$ (greater than about 1 V). Since this drives Q3 out of saturation and I_B is held constant, I_{SK} (the current into the output terminal) is proportional to h_{FE}.

If sufficient I_{SK} data were available for lot-to-lot and manufacturer-to-manufacturer variations for each of the TTL families, the data could be converted to K_D and statistically characterized to yield a neutron design margin (NDM) as was done for the transistors. If the variation in electrical parameters of the constituent transistors were known, the transistor worst-case model could be used to calculate an upper bound for K_D. In the absence of this information, we assume that the variations encountered in TTL devices will be less than those encountered in discrete transistors. Therefore, the NDM values of table III (obtained for discrete devices) can be used as a conservative value for TTL devices.

For TTL devices a fan-out of ten is the most sensitive condition. As the fan-out decreases the forced h_{FE} (h_{FEF}) decreases because it is directly proportional to collector current. In other words, if the fan-out drops from 10 to 5 (a factor of 2), the threshold fluence for the standard TTL family increases by a factor of 2. This rule-of-thumb must be applied with some caution (especially to flip flops) because it is possible for an internal gate to fail before the output gate.

Assuming a constant $I_{B(MIN)}$, which is calculated from circuit analysis of the output TTL gate stage, the category II criterion is

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC}$$

where the NDM is obtained from table III at the desired P_F and Φ_{MF} is given by

$$\Phi_{MF} \geq \frac{2\, f_{T(MIN)}}{(0.8)(10^{-6})}\; I_{B(MIN)}\left[\frac{1}{I_{SK(FAIL)}} - \frac{1}{I_{SK(MIN)}}\right] \quad . \text{(C3)}$$

This criterion assumes that the TTL device will fail because of the output gate and not an internal gate. This is more true for the large fan-out case than it is for the small fan-out case because the output gate safety margin is lower under high fan-out. Unless a better estimate is available, $f_{T(MIN)}$ can be replaced by 250×10^6 Hz and I_{SK} by the values given below (depending on the fanout).

Estimated $I_{SK(FAIL)}$	Fan-Out
25 mA	10
12 mA	5
5 mA	2
2.5 mA	1

C-3.0 PROCUREMENT SPECIFICATIONS FOR HARDNESS ASSURANCE

Several techniques have been proposed for TTL circuits relating various electrical screens to the prediction of neutron effects, but limitations exist on all of them as can be seen in table C-1. None of the techniques appears to provide the same effective neutron response prediction information developed earlier for transistors without making some modification to the structure of the device for access to each critical element. Of the candidate screens listed in table C-1, I_{SK} appears to be the best.

Johnston and Skavland [4] propose a terminal (V_{OH}) measurement technique that uses the difference between the power supply voltage and the output high (modified input conditions) voltage to provide an effective screening parameter for the neutron response of TTL IC's. The requirements on this technique are that the chip circuit design and internal transistor geometry be known and fixed.

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[4] Johnston and Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trans. Nucl. Sci,. NS-22, 2303, Dec. 1975

TABLE C-1. CANDIDATE TRANSISTOR-TRANSISTOR LOGIC SCREENING AND QUALITY CONFORMANCE PARAMETERS.

Parameter	Advantages	Limitations
I_{SK} (output sink current)	(1) Gain margin of output transistor can be established (2) I_{SK} is easily measured (3) I_{SK} degrades in a manner similar to h_{FE} of individual transistor	(1) V_{BE} and $V_{CE(SAT)}$ variations not included (2) Gain measured at fixed base current (collector current will vary (3) Resistor ratio process variation not included
V_{OH}, (terminal V_{BE})[a]	(1) A dc measurement (2) Applicable to most TTL devices (3) No special metallization patterns required (4) A good screening parameter	(1) Circuit design needs to be fixed (2) Transistor geometries need to be fixed (3) Leakage currents not included
TPLH and TPHL	(1) f_T of the phase-splitter and output transistors can be estimated (2) Useful for more complex circuits	(1) Switching time tends to be dominated by output load capacitance (2) f_T measurements are not easily made (3) Requires special metallization pattern
V_{OL}		(1) Changes in this parameter are small, so measurements must be very accurate

[a]A. Johnston and R. Skavland, Terminal Measurements for Hardness Assurance in TTL Devices, IEEE Trans. on Nucl. Sci., NS-22, 2303, December 1975.

Changes in switching times of TTL devices after neutron exposure can also be related to transistor h_{FE} degradation, however the behavior of these two parameters is strongly nonlinear with neutron fluence. TLPH is the propagation delay time, low to high level, and is defined as the time between the specified reference points in the input and output voltage waveforms with the output changing from the defined low level to the defined high level. The TPHL is the propagation delay time, high-to-low-level output. Switching times can yield an estimation of the f_T of the phase splitter and output transistors; however, low correlation with neutron damage[3] reduces the effectiveness of this parameter as an HA screen.

[3]Johnston and Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci., NS-21, 393, December 1974.

Another approach to the HA problem is the use of devices with special leads to allow direct access to the base of the output transistor.[5] However, variations in transistors across a wafer may be severe enough that the output transistor may not accurately predict the worst-case element degradation for anything larger than a simple small-scale integration IC. This technique, however, may be the only option available for complex IC's. Breakout transistors could be used, but care must be taken so that the transistor selected has the lowest gain-bandwidth product and the largest area of any elements in the device itself.

The output low-level voltage (V_{OL}) degrades nonlinearly with neutron fluence. The problem of predicting post-irradiation V_{OL} is analogous to the $V_{CE(SAT)}$ problem of discrete transistors.

A Procurement Specification example for the SN5400 TTL gate is given in table C-2. A screen on I_{SK} for control level 2 and 1 devices is shown because it has had some success in sorting out softer units. Insufficient data preclude the establishment of a benefit/cost ratio for this screen; however, it is expected to follow the less-than-one value of the transistor. Thus, this screen should only be imposed as a last resort.

Radiation quality conformance testing should be done for

$$\frac{\Delta\ 1/I_{SK}}{\Phi}$$

which is analogous to the K_D case for transistors.

C-4. HARDNESS ASSURANCE PROCUREMENT EXAMPLE

Suppose that an SN5400 NAND gate is to be used in a circuit with the following requirements:

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[5] I. Arimura, A Study of Electronics Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory, Albuquerque, NM, AFWL-TR-73-135, January 1974.

TABLE C-2. EXAMPLE PROCUREMENT SPECIFICATION FOR TRANSISTOR-TRANSISTOR LOGIC NAND GATES

Hardness assurance control	Parameter	Test method	Test condition	Control level failure criterion S-2 Min	S-2 Max	S-1 Min	S-1 Max	Units
Process controls	Base width and resistivity profile	TBD[a]	-	-	TBD	-	TBD	-
	configuration	-	-	-	-	-	-	-
Screens	I_{SK}	ASTM 11A21	TBD	TBD	-	TBD	-	mA
Radiation quality conformance test[b]	$\Delta(1/I_{SK})$	ASTM 11A21	TBD	-	-	-	TBD	mA

[a]TBD means to be determined.

[b]Radiation tests are read-and-record on 10 samples at three neutron levels which cause 20%, 50%, and 80% degradation in the reciprocal sink current $(1/I_{SK})$.

a. fan-out = 10,

b. $\Phi_{SPEC} = 5 \times 10^{13}$ neutrons per square centimeter,

c. $P_F = 1 \times 10^{-4}$ at 90 percent confidence.

The HA requirements are obtained from the procedure illustrated in figure 1.

Step 1. Determine if Φ_{TH} is greater than Φ_{SPEC}. Φ_{TH} for TTL circuits is the fluence at which constituent transistors start to degrade. This fluence was established in section 2 at 1×10^{10} n/cm^2. Since Φ_{SPEC} is above this level, proceed to step 2.

Step 2. Determine if HA is necessary. Circuit analysis of the SN5400 yields an I_B of 3 mA for the lower output transistor calculated from equation C1. TTL logic at a fan-out pf 10 requires the output transistor to sink at least 25 mA of current. The h_{FEF} is thus 25/3 or 8.3. The h_{FE} at which the output transistor will start to come out of saturation ($h_{FE(FAIL)}$) is about $(1.3)(h_{FE})$ or 10.8. The minimum gain-bandwidth product ($f_{T(MIN)}$) is 250 MHz.[3] Assuming that $1/h_{FE(MIN)}$ is negligible in comparison with $1/h_{FE(FAIL)}$, the category II criterion is given by

$$\Phi_{MF} \geq \Phi_{SPEC}$$

where

$$\Phi_{MF} \geq \frac{2\pi\ f_{T(MIN)}}{0.8 \times 10^{-6}}\ 1/h_{FE(FAIL)} \quad .$$

Substitution of the values for $f_{T(MIN)}$, $h_{FE(FAIL)}$ and the NDM from table III yields a value of 2.5×10^{13} n/cm^2, which is less than Φ_{SPEC}, so proceed to step 3.

Step 3. If HA is necessary, procure an S-1 control part and perform accept/reject testing. There are two ways to gather the statistical data needed to make the accept/reject decision. One way is to select the electrical parameter of interest, calculate the value of the parameter at which circuit failure will occur, and then perform a statistical analysis on the failure fluence data. This method is identified in appendix F as case 2, and the disadvantage of this approach is that parameter degradation is usually nonlinear with fluence, which makes statistical extrapolation to low probabilities of failure risky.

The second method (case 1 in appendix F) of gathering the statistical data needed to make the accept/reject decision is to use I_{SK} as a

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[3] Johnson and Skavland, Neutron Hardness Assurance Techniques for TTL Integrated Circuits, IEEE Trans. Nucl. Sci., NS-21, 393, December 1974.

means of obtaining h_{FE} of the output transistor. Then the previously explained method for transistors can be used. The advantage with this method is that $\Delta 1/h_{FE}$, and consequently, ΔI_{SK}, degrades linearly with fluence.

Using the second method, suppose a random sample of 10 SN5400 units were chosen from a production lot and subjected to neutron fluence testing. The 10 sample I_{SK} data can be converted to $\Delta 1/h_{FE}$ data using equation C1 with I_B calculated from equation C2. From this $\Delta 1/h_{FE}$ data the statistical distribution of $\ell n\ K_D$ can be obtained. Suppose the 10 sample data had a mean ($\overline{\ell n\ K_D}$) of -36.15 with a sample standard deviation (s_{LN}) of 0.2. The K_D corresponding to a P_F of 1×10^{-4} at 90 percent confidence can be calculated from equation 6 to be 5.9×10^{-16} cm^2/n. Assuming that $1/h_{FE(MIN)}$ is negligible when compared with $1/h_{FE(FAIL)}$, the Φ_F is given by

$$\Phi_F = \frac{1}{5.9 \times 10^{-16}} (1/10.8)$$

$$= 1.57 \times 10^{14}\ n/cm^2,$$

where $h_{FE(FAIL)}$ is the 10.8 value calculated in step 2. Since the Φ_F is greater than Φ_{SPEC}, the lot can be accepted.

APPENDIX D
OPERATIONAL AMPLIFIER HARDNESS ASSURANCE

D-1. TYPES OF OPERATIONAL AMPLIFIERS

One of the main differences between linear and digital IC's is the internal device current dependence on complex current sources. Each type of operational amplifier (op amp) uses somewhat different current sources and so to go into a detailed circuit analysis of each of the many types is beyond the scope of this effort. In this section only the LM101A, the 741, and LM108A types of op amps will be examined in detail to show the general application of the HA methodology.

D-1.1 TYPE LM101A

The LM101A, [1] announced in 1967, was a major advance over the 708, which was the first monolithic op amp to be mass produced. A circuit schematic of the LM101A is given in Figure D-1. The NPN emitter followers Q1 and Q2 are the input transistors. They drive the lateral PNP transistor Q3 and Q4, which are connected in a differential common base configuration. Q5 and Q6 serve as collector loads for the input stage. The second-stage amplifier Q10 uses Q17 as an active load. [2] The emitter followers Q7 and Q9 increase the overall current gain. A class AB output stage is provided by the lateral PNP Q12 and the NPN Q11. Q14 and Q13 eliminate the dead zone in the output stage. Note that the 101A does not use the vertical PNP transistor structure.

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[1] R. Widlar, Monolithic Op Amp with Simplified Frequency Compensation, EEE, 15, 58, July 1967.

[2] R. Widlar, Design Techniques for Monolithic Amps, IEEE J. Solid State Circuits, SC-4, 184, August 1969.

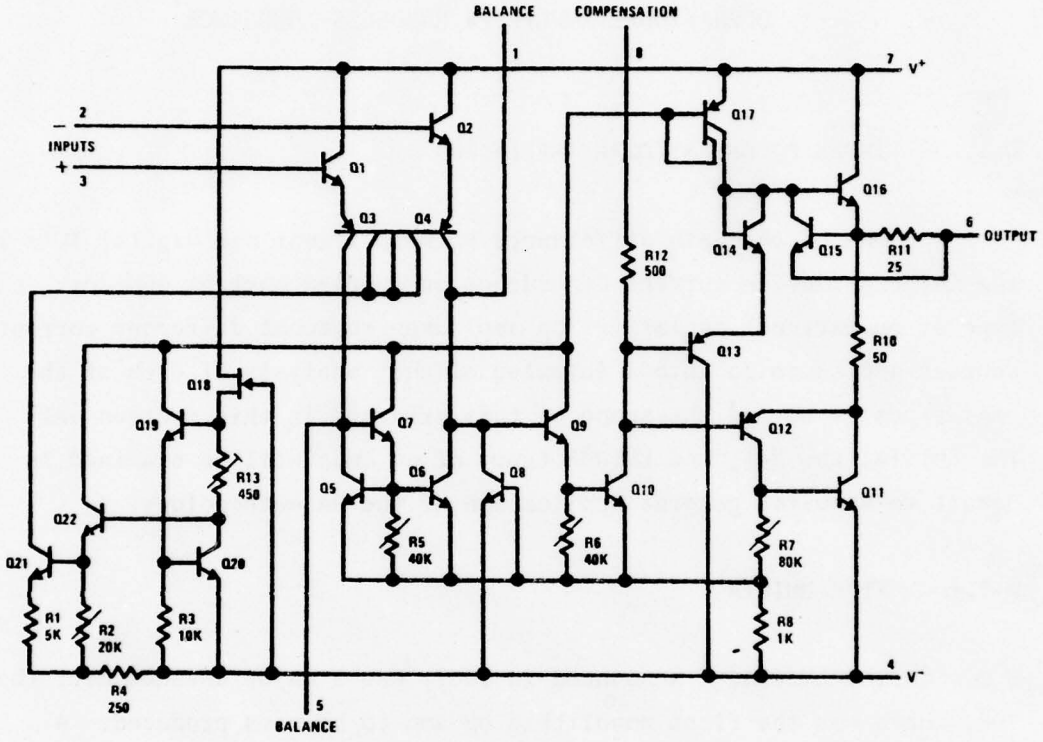

Figure D-1. Type LM101A operational amplifier.

D-1.2 Type 741

The 741 put the LM101A compensation capacitor on the silicon chip and used a vertical PNP transistor structure in the Class AB output stage. A schematic of the 741 is given in Figure D-2.

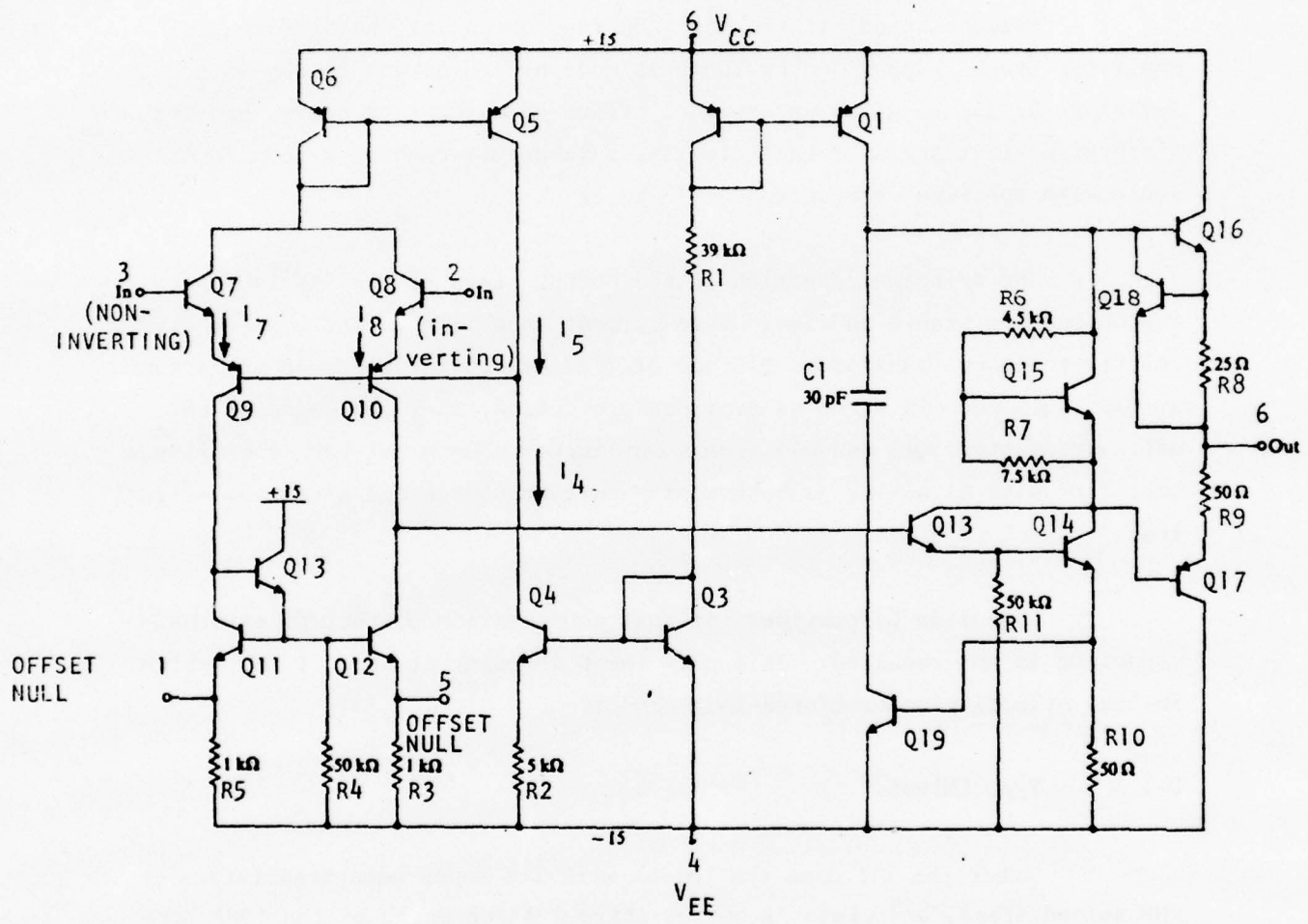

Figure D-2. Type 741 operational amplifier.

The 741 input stage employs a differential amplifier (Q7, Q8, Q9, Q10) which uses an active load (Q11, Q12, Q13) to develop high gain. Transistors Q7 and Q8 operate in the common collector mode and Q9 and Q10 in

the common base mode. Q9 and Q10 act as level shifters to isolate the input from the power supply voltages V_{CC} and V_{EE}. The differential amplifier output comes from the collectors of Q10 and Q12. Transistors Q1, Q2, Q3, Q4, Q5, and Q6 are used for biasing purposes. The emitter currents (I_7 and I_8) remain essentially unchanged at 15 μA for wide variation in lateral PNP beta.[3]

Feedback stabilization of the bias current of the differential amplifier stage is provided by the bias current source comprising Q5 and Q6. Resistors R3 and R5 allow an external offset adjustment to compensate for differences in transistor characteristics (a pot is connected to pins 1 and 5 with the wiper connected to -15 Vdc).

The principal function of the output stage of the 741 is to provide low output resistance and large load current capability. The complementary emitter follower transistors Q16 and Q17 are biased for Class AB operation by Q15. Q18 and Q19 serve as overload protection, they are normally cut off. Transistors Q13 and Q14 form a Darlington common emitter second-stage amplifier with Q1 acting as both a bias current source and as a small-signal load.[3]

Capacitor C1 provides internal compensation so that an external capacitor is not required. This puts the 0 dB point at about 1 MHz, which insures stability under closed-loop condition.

D-1.3 Type LM108A

After the 741 came the LM108A with its super beta transistors, PNP second stage, and class AB output stage. A schematic of the 108A (the 308 is the commercial version) is given in Figure D-3.[4]

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[3]D. J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill, 1975.

[4]R. Widlar, National Semiconductor Application Note, AN-29, December 1969.

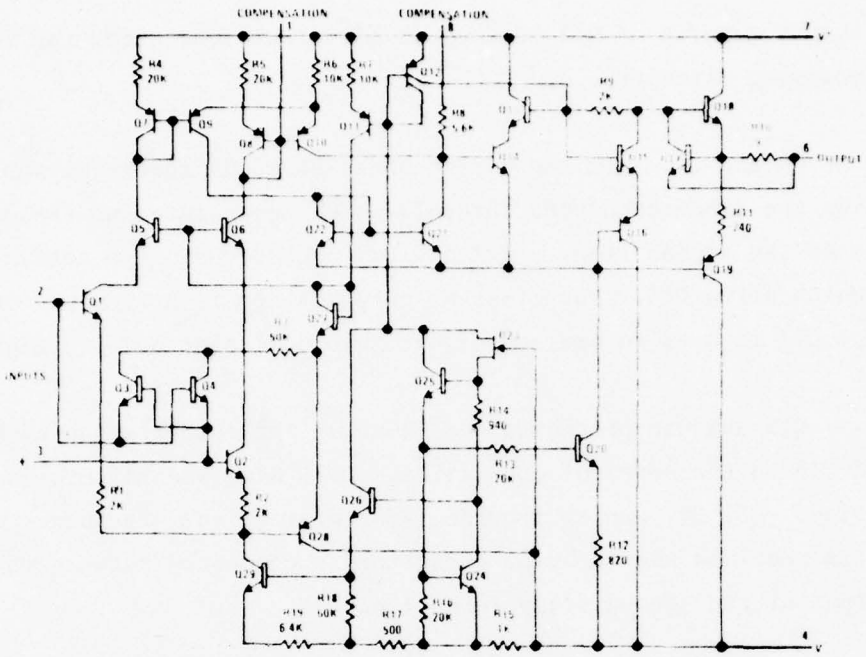


Figure D-3. Type LM108A operational amplifier.

In Figure D-3 the super gain NPN transistors ($\beta \sim 5000$ and 4V breakdown voltage) are differentiated from the standard NPN transistors by drawing the standard units with a wider base. Q16 and Q19 are vertical (substrate) PNP transistors. Q9 and Q10 are high-gain lateral PNP transistors ($\beta \sim 150$ and 80V breakdown voltage) and form the second stage differential amplifier. Q23 is a FET with a saturation current of about 30 μA, which is used to establish the collector current for Q24. The FET provides the initial turn-on current for the circuit.

The input super gain transistors Q1 and Q2 are operated in a cascode connection with Q5 and Q6. The bases of Q5 and Q6 are bootstrapped to the emitter of Q1 and Q2 through Q27 and Q28 so that the input transistors are operated at zero collector-base voltage. Q29 provides a total input stage current of 6 μA at 25 C. The output currents of Q23, Q24, Q25, and Q26 are fed to Q12 which in turn is connected to Q11. The

15 μA output current of Q11 is used as a current source for the input stage boot-strapping circuitry.

Q9 and Q10 form the basic second-stage differential amplifier. Q7 and Q8 are diode-connected laterals which compensate for the emitter-base voltage of the second stage. Q21 and Q22 are second stage active collector loads which drive Q14. The class AB output stage is driven by the emitter of Q14. Q13 is used to operate Q14 at zero collector-base voltage.

Q15 and Q16 prevent a dead zone in the output stage by biasing Q18 and Q19 on the verge of conduction. Q17, R10, and R11 provide output protection. Q3, Q4, and R3 provide input protection. Frequency compensation is provided when a 30 pF capacitor is connected between the input and output of the second stage (pins 1 and 8).

D-1.4 Operational Amplifier Transistor Structures

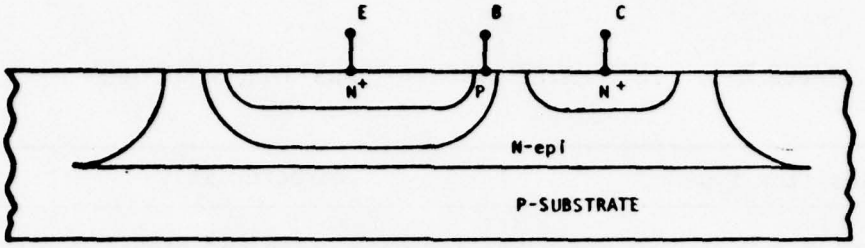
Four general types of transistors can be encountered in commercial bipolar op amp designs: (1) normal NPN transistors, (2) super-gain NPN transistors, (3) lateral PNP transistors, and (40 vertical (substrate) PNP transistors.[5] The sensitivity of these individual devices to neutron damage varies widely because of differences in topology, doping levels, and base width. Table D-1 lists the relevant characteristics of the four transistor types; figure D-4 gives a comparison of the structure.

Lateral PNP transistors have lower gain and suffer more neutron damage than other NPN and PNP constituent transistors. This is because the lateral PNP transistor is a wide base device owing to masking tolerances and side-wall diffusion. Johnson[5] gives a mean lateral PNP damage factor of 3.5×10^{-14} and shows a tighter distribution than the NPN transistors. The mean K_D for the worst lot for the NPN input transistor for 38510 versions of the 741 was 0.7×10^{-14} cm^2/n.[5] Vertical (substrate) PNP transistors

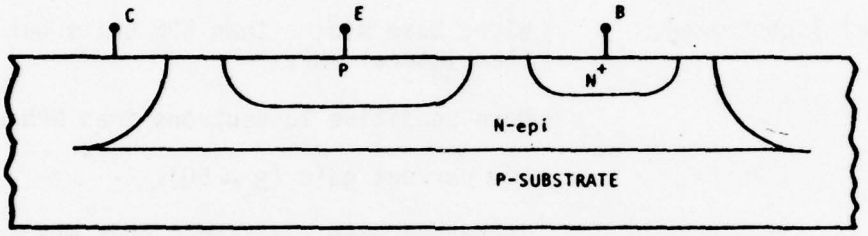
[5] A. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci., NS-24, 2071, December 1977.

TABLE D-1. INTEGRATED CIRCUIT TRANSISTOR STRUCTURE

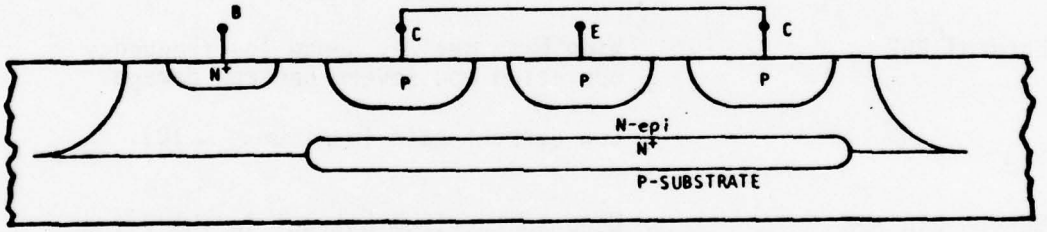
Transistor type	Characteristic
Standard NPN	Smaller base width and higher gain (30-100) than PNP transistor.
	Less sensitive to neutrons than PNP units.
Vertical (substrate) PNP	Wider base widths than NPN units but smaller than lateral PNP.
	More sensitive to neutrons than NPN units.
	Low current gain ($\beta \sim 50$).
	Increased base resistance over NPN means lower onset of current crowding.
	Useful as emitter followers.
Lateral PNP	Wide base device, hence low-frequency operation and severe neutron damage.
	Low current gain (maximum $\beta \sim 10$).
Super-gain NPN	Used in the 108A but not in the 741 or 101A.
	Increases input resistance and lowers input bias current.
	Special circuit design required to prevent punch-through.
	Base width less than 0.1 μm and β greater than 2000.
	Requires an extra emitter diffusion.



(a) Standard NPN IC transistor.



(b) Vertical (Substrate) PNP transistor.



(c) Lateral PNP transistor.

Figure D-4. Transistor cross sections: (a) standard NPN integrated circuit, (b) vertical (substrate) PNP, and (c) lateral PNP. From D.J. Hamilton and W. G. Howard, Basic Integrated Circuit Engineering, McGraw-Hill, 1975.

have a smaller base width than the lateral PNP devices and are thus less sensitive to neutron effects (but are still more sensitive than NPN devices).

D-2. EFFECTS OF NEUTRON RADIATION

Op amps have a number of electrical parameters which are critical in most applications. These are the open-loop voltage gain (A_{VOL}), the input bias current (I_B), the input offset current (I_{OS}), the input offset voltage (V_{OS}), the common-mode rejection ratio (CMRR), the slew rate (SR), and the output current (I_{SS}). These terms are defined in table D-2. The 101A, 741, and 108A specifications for some of these parameters are presented in table D-3.

TABLE D-2. OPERATIONAL AMPLIFIER DEFINITIONS

Term	Definition
Large signal voltage gain	Ratio of maximum output voltage swing to change in input voltage required to drive output to this *voltage*
Input bias current	Average of two input currents at 0 output voltage
Input offset current	Difference in currents into two input terminals with output at 0 V
Input offset voltage	That voltage which must be applied between input terminals to obtain 0 *output voltage*
Common mode rejection ratio	Ratio of change of input offset voltage to input common mode voltage change producing it (decibels)
Slew rate	Maximum rate of change of output voltage under large-signal conditions
Output short-circuit current	Maximum output current available from amplifier with output shorted to ground or to either supply
Supply current	Current required from power supply to operate amplifier with no load and zero output

TABLE D-3. OPERATIONAL AMPLIFIER SPECIFICATIONS

Parameter	Test condition (T_A = 25°C)	Device type	Min	Max
Input offset voltage	R_S = 50 Ω 883B-4001	741 LM101A LM108A	– – –	5.0 mV 2.0 mV 0.5 mV
Input offset current	883B-4001	741 LM101A LM108A	– – –	200 nA 10 nA 0.2 nA
Input bias current	883B-4001	741 LM101A LM108A	– – –	500 nA 75 nA 2 nA
Output short-circuit current	$+V_{CC}$ = 15 V 883B-4001	741	–	35 mA
Supply current	$+V_{CC}$ = ±15 V 883B-4005	741 LM101A LM108A	– – –	2.8 mA 3.0 mA 0.6 mA
Large signal voltage gain	$\pm V_{CC}$ = 15 V, R_L = 2 K V_{OUT} = ±10 V 883B-4004	741 LM101A LM108A	50 V/mV 50 V/mV 80 V/mV	– – –

For most op amps the sensitive electrical parameters to neutron irradiation are I_B, I_{OS}, A_{VOL}, V_{OS} and I_{SS}. In general, I_B increases with neutron fluence, A_{VOL} decreases, and I_{SS} decreases, but I_{OS} and V_{OS} go either way. Significant changes in V_{OS}, I_{OS}, and I_{SS} do not usually occur until after significant degradation of other parameters has taken place. For example, after 2.3×10^{12} n/cm^2 a typical 741 has experienced a 5% change in V_{OS}, a 65% change in I_{OS}, and a 300% rise in I_B.[5] Therefore the increase of I_B or the decrease in A_{VOL} is the most sensitive indicator of radiation damage.

The open-loop gain degrades with neutron fluence but it does not change in a smooth predictable way. In addition, the measurement and interpretation of the open loop gain is not straightforward. The open-loop voltage gain must be carefully measured and defined if meaningful

[5] A. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci., NS-24, 2071, December 1977.

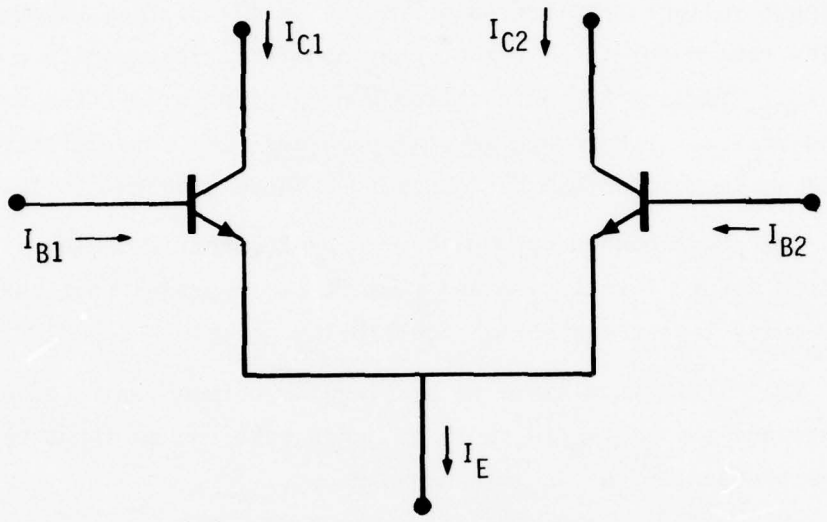


Figure D-5. Operational amplifier differential input stage equivalent circuit.

$$1/h_{FE1} = \frac{I_{B1}}{I_{C1}} \tag{D3}$$

$$\Phi K_{D1} = 1/h_{FE2(rad)} - 1/h_{FE1(0)} \tag{D4}$$

$$\Phi K_{D2} = 1/h_{FE2(rad)} - 1/h_{FE2(0)} \quad . \tag{D5}$$

Adding equations D4 and D5 and using D3,

$$\Phi(K_{D1} + K_{D2}) = \frac{I_{B1(rad)}}{I_{CI(rad)}} + \frac{I_{B2(rad)}}{I_{C2(rad)}} - \left(\frac{I_{B1(0)}}{I_{C1(0)}} + \frac{I_{B2(0)}}{I_{C2(0)}}\right) \tag{D6}$$

Substituting $I_{E/2}$ for I_{C1} (equation D2)

$$(K_{D1} + K_{D2})\Phi = \frac{4I_{B(rad)}}{I_{E(rad)}} - \frac{4I_{B(0)}}{I_{E(0)}} \tag{D7}$$

interpretations are required of the degradation of this parameter in irradiation environment. The best approach is to measure the transfer characteristic in a loaded and unloaded condition and define the gain in terms of the *maximum* input voltage required to drive the output voltage through a given range. The reason for this is that many manufacturers specify a dc measurement for A_{VOL}, forcing the output from a negatrive to positive voltage with a fixed load-resistor. However, several problems with this definition make it unsuitable as is pointed out by Johnston.[6] These problems follow:

(1) Most modern op amps have a 3-dB corner frequency in the 1 to 10 Hz region before irradiation and thus it is important that the test time be sufficiently long to establish equilibrium.

(2) It is impossible to distinguish between small drifts in offset voltage and the small (10 to 15 mV) change in the dc input voltage which is expected for the dc gain measurement.

(3) The output stage has a significant effect on the open-loop gain. The gain is a function of the load conditions and there is a large difference in the gain between loaded and unloaded conditions. The gain in the loaded condition is also very nonlinear, which confuses the definition of gain and allows contradictory results.

Changes in I_B are important in usual op amp applications. Since I_B is very radiation sensitive, it is a good indicator of the onset of significant damage. For low neutron fluences ($\lesssim 10^{12}$) the change in I_B with fluence is approximately linear because I_B is the input transistor base current. For the simplified equivalent op amp circuit of figure D-5,

$$I_B = \frac{I_{B1} + I_{B2}}{2} \qquad \text{(D1)}$$

$$I_E \cong I_{C1} + I_{C2} \qquad \text{(D2)}$$

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[6] A. Johnston, Hand Analysis Techniques for Neutron Degradation of Operational Amplifiers, IEEE Trans. Nucl. Sci., NS-23, 1709, December 1976.

For the LM108A at low fluences $I_{E(rad)} \approx I_{E(0)}$, so

$$(K_{D1} + K_{D2})\Phi = \frac{4}{I_{E(0)}} \Delta I_B \quad . \tag{D-8}$$

This last approximation is valid for the LM108A because of weak dependence of I_E on lateral PNP common base gain (α). It is less valid for the 741 and 101A because I_E for the 741 is directly dependent on α, and I_E for the LM101A is dependent on α^2.[D5]

I_E is measured at the balance terminal (pin 1) for the externally compensated LM108A. For internally compensated units such as the 741, the measurement cannot be made on the standard package; either a special lead needs to be brought out to the unused pin 8 on the package or I_E needs to be estimated from the slew rate.[5] The input stage current of the 741 ($I_7 + I_8$ in Figure D-2) is derived from the collector of Q6. The Q5 collector current (I_5 in Figure D-2) also is equal to ($I_7 + I_8$) which in turn is approximately equal to I_4, the stabilized current. Thus, any point which allows the monitoring of ($I_7 + I_8$) can be brought out to pin 8 for HA monitoring.

D-3. CATEGORY II CRITERION

The threshold fluence (Φ_{th}) for the worst case transistor model was calculated in section 2 to be 1×10^{10} n/cm^2. Since the neutron response of an op amp is a combination of the response of its constituent transistor parts, the Φ_{th} of 1×10^{10} n/cm^2 is also valid for op amps.

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[5] A. Johnston, Application of Op Amps to Hardened Systems, IEEE Trans. Nucl. Sci. NS-24, 2071, December 1977.

From equation D-8, assuming identical input transistors,

$$\left(\frac{K}{2\pi f_T}\right)\Phi = \frac{2}{I_{E(0)}}\left[I_{B(rad)} - I_{B(0)}\right] \tag{D9}$$

where K_D has been replaced by $K/2\pi f_T$ (see equation 2). The mean failure fluence Φ_{MF}, is given by

$$\Phi_{MF} = \frac{4\pi f_T}{I_{E(0)}K}\left[I_{B(FAIL)} - I_{B(0)}\right] \tag{D10}$$

where the application-failure input bias current, $I_{B(FAIL)}$, is replaced by $I_{B(rad)}$. Replacing f_T with a minimum value, $I_{B(0)}$, with a maximum value from the manufacturer's data sheets ($I_{B(MAX)}$) and $I_{E(0)}$ with a maximum value obtained from a characterization sample yields a minimum estimate of Φ_{MF} in a manner similar to the discrete transistor analysis of section 2.2

$$\Phi_{MF} \geq \frac{4\pi f_{T(MIN)}}{I_{E(MAX)}K}\left[I_{B(FAIL)} - I_{B(MAX)}\right] \tag{D11}$$

Unless better estimates are available, $f_{T(MIN)}$ can be replaced with 250×10^6 Hz and K by the low injection value of 7×10^{-6} $cm^2/n{\cdot}s$. $I_{E(MAX)}$ can be replaced by 10 μA for the LM108A, by 40 μA for the LM101A, and 20 μA for the 741. Equation D-11 must be used with caution because it was developed for low fluences where I_E does not change significantly.

Using equation D-11, the values given above for $f_{T(MIN)}$ and $I_{E(MAX)}$, and a failure criterion of 2 $I_{B(MAX)}$, a minimum Φ_{MF} value can be calculated for each of the three types of op amps. For the LM308A,

$$\Phi_{MF} \geq \frac{4\pi(250\times10^6)}{(10\times10^{-6})(7\times10^{-6})}\left[2I_{B(MAX)} - I_{B(MAX)}\right]$$

$$\geq 3 \times 10^{11}\ n/cm^2$$

using the 7 nA $I_{B(MAX)}$ value from the data sheets. In a similar manner,

a minimum estimate of Φ_{MF} can be calculated for the 101A

$$\Phi_{MF} \geq \frac{4\pi(250\times10^{6})}{(40\times10^{-6})(7\times10^{-6})} \left[75 \times 10^{-9}\right]$$

$$\geq 1 \times 10^{12} \text{ n/cm}^2.$$

For the 741,

$$\Phi_{MF} \geq \frac{4\pi(250\times10^{6})}{(20\times10^{-6})(7\times10^{-6}} \left[500 \times 10^{-9}\right]$$

$$\geq 1 \times 10^{13} \text{ n/cm}^2$$

using the $I_{B(MAX)}$ values in table D-3.

In the absence of a large body of statistical data representing manufacturer-to-manufacturer and lot-to-lot variation, the NDM values of table III for discrete transistors will be used. This assumes that the variation in op amps will be less than that encountered in discrete transistors.

The category II criterion for op amps is thus

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC}$$

where Φ_{MF} is obtained from

$$\Phi_{MF} \geq \frac{f_{T(MIN)}}{I_{E(MAX)}K} \left[I_{B(FAIL)} - I_{B(MAX)}\right]$$

and is roughly 3×10^{11} for the LM308A, 1×10^{12} for the 101A, and 1×10^{13} n/cm^2 for the 741.

The NDM is obtained from table III at the desired P_F at 90 percent confidence. The category II criterion at a P_F of 10^{-4} (an NDM of 6.8 obtained from table III) is thus a ϕ_{SPEC} of 5×10^{10} for the LM308A, 1×10^{11} for the LM101A, and 1×10^{12} for the 741 based on these rough estimates.

D-4. PROCUREMENT SPECIFICATIONS FOR HARDNESS ASSURANCE

Several HA screens have been proposed for 741 op amps. These include:

(1) measurement of the first stage bias current (I_{10}) with a screen to dischargd devices with abnormally low ro high values of bias current,[5]

(2) specification and measurement of the open-loop voltage gain (A_{VOL}) with a screen to discard devices with abnormally low values.[8]

In addition, two special methods have been proposed: (1) special leads for the output transistor[8] and (2) a high-frequency ac probe wafer measurement.[9] In the latter method, a commercially available high frequency ac probe is used for making measurements on the elements of the integrated circuits on the wafer. This can be used as a 100 percent screen of the elements in an IC or on breakout transistors. It is used in the early stages of the manufacturer's process. Basically, the technique measures the minority carrier delay time of each transistor element with a temporary metallization pattern. The temporary pattern is removed after the measurement and an operational pattern is then applied. In this technique the silicon damage constant is assumed to be constant with current and the total minority delay time is obtained

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[5] A. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci., NS-24, 2071, December 1977.

[8] I. Arimura, A Study of Electronic Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory, AFWL-TR-73-134, January 1974.

[9] R. A. Bailey, et al., A Neutron Hardness Assurance Screen Based on High Frequency Probe Measurements, IEEE Trans. Nucl. Sci., NS-23, 2020, December 1976.

from S parameter measurements. By applying this technique at the wafer stage, significant savings were realized through eliminating IC's with poor radiation performance before the costly packaging stage. This was found to be especially true for higher reliability IC's and hybrids where the package level yield can be quite low.

Special leads attached to the output transistor have also been proposed as a possible HA tool. Since the output transistor uses the same process sequence for base doping and base width, an extra lead or two may provide the necessary parameters for worst-case predictions and comparisons of IC's. The problem with examining only the output transistor is that both PNP and NPN transistors are on the same monolithic chip and the PNP units have a different damage constant. The PNP units control the input differential stage emitter current and, since K_D varies with current, the PNP devices can cause significant device degradation.

Johnston[5] has suggested a screen on the first stage emitter current (I_E) as a means of reducing the ΔI_B due to neutron damage for low neutron fluences. Since the input boas current is the base current of the bipolar transistor differential stage, we have already seen that

$$\frac{I_{B(rad)}}{I_E} = \frac{I_{B(0)}}{I_E} + \frac{K_D}{2} + \Phi.$$

Thus, a screen to remove those operational amplifiers with the highest $I_{B(0)}/I_E$ ratio will result in a harder distribution in the same manner in which the $h_{FE(MIN)}$ screen did for transistors.

I_E is measured in the following way for each of the three operational amplifiers.

- 108A - Pin 1 to V_{CC}
- 101A - Pin 5 to V_{EE}
- 741 - Slew rate

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[5] A. Johnston, Application of Operational Amplifiers to Hardened Systems, IEEE Trans. Nucl. Sci., NS-24, (December 1977), 2071.

The 741 is internally compensated, so a direct measurement of I_E cannot be made on a standard pin-out. The slew rate is used instead because it is approximately proportional to I_E.

Table D-4 is an example of an operational amplifier procurement specification. An electrical screen on I_B/I_E is recommended, although the cost-effectiveness of this screen should be examined. Radiation lot-sample testing is accomplished by obtaining a distribution of failure fluences using circuit application-defined parameter failure criteria.

TABLE D-4. EXAMPLE PROCUREMENT SPECIFICATION FOR OPERATIONAL AMPLIFIERS

Hardness assurance control	Parameter	Test method	Test condition	Control level failure criterion S-2 Min	S-2 Max	S-1 Min	S-1 Max	Units
Process control	Base width and resistivity profile	TBD[a]	TBD	-	TBD	-	TBD	cm^{-3}
Screen	I_B/I_E	TBD	TBD	TBD	TBD	TBD	TBD	-
Radiation quality conformance test	Φ_F	MIL-STD-883B-1017[b]	TBD	-	-	TBD	-	n/cm^2

[a]TBD means that it is to be determined, I_B is the input bias current, I_E is the differential stage emitter current, and Φ_F is the application-defined failure fluence at a given probability of failure.

[b]MIL-STD-883B is titled Test Method and Procedures for Integrated Circuits.

D-5. HARDNESS ASSURANCE PROCUREMENT EXAMPLE

Suppose for this example that the LM308A operational amplifier was desired in a certain application. The application failure criteria are

$$\Phi_{SPEC} = 5 \times 10^{11},$$

$P_F = 1 \times 10^{-4}$ at 90 percent confidence,

A_{VOL} = 6 Mininum,

I_B = 7 nA Maximum,

I_{OS} = 10 nA Maximum,

V_{OS} = 1 mV Maximum.

We now follow the procedure of figure 1.

Step 1. Determine if Φ_{TH} is greater than Φ_{SPEC}. Since Φ_{TH} for operational amplifiers is 1×10^{10} n/cm^2, the preceding statement is not true and we must proceed to level 2 in figure 1.

Step 2. Determine if HA is necessary. The category criterion is given by

$$\frac{\Phi_{MF}}{NDM} \geq \Phi_{SPEC}$$

where a minimum estimate of Φ_{MF} was obtained for the LM308A from equation D11 to be 3×10^{11} n/cm^2. At a P_F of 1×10^{-4} table III yields an NDM of 6.8. Thus, since $(3 \times 10^{11})/(6.8)$ is 4.4×10^{10}, which is less than the Φ_{SPEC} of 5×10^{11}, proceed to step 3.

Step 3. If HA controls are necessary, procure an S-1 control lot and perform accept/reject testing. Suppose one lot of 30 LM308A op amps were purchased and a random sample of 10 devices from the lot were subjected to neutron exposures of 2×10^{12}, 5×10^{12}, and 1×10^{13} n/cm^2. Examination of table D-5 shows that of the op amp neutron sensitive parameters I_B is the only one that does not have an order-of-magnitude margin between the application failure criteria and the minimum/maximum values of the sample at 10 Φ_{SPEC}. Thus, the failure fluence Φ_F is that fluence at which I_B

TABLE D-5. LM308A CRITICAL PARAMETER SPECIFICATIONS

Critical parameter	Manufacturer's specification		Example failure criterion		Sample of 10 Values after 10 Φ_{SPEC}		Units
	Min	Max	Min	Max	Min	Max	
Open loop gain (A_{VOL})	60	–	6	–	54	–	V/mV
Input bias current (I_B)	–	7	–	7	–	11	nA
Input offset current (I_{OS})	–	1	–	10	–	.7	nA
Input offset voltage (V_{OS})	–	.5	–	10	–	1.5	mV

is 7 nA and is calculated in table D-6 by linear extrapolation. The $\ell n \Phi_F$ data cumulative frequency distribution is shown in figure D-6 to be approximately lognormal with a $\ell n \Phi_F$ mean of 29.06 and a sample standard deviation of 0.27. From equation 6 the estimate of the lot Φ_F at a P_F of 1×10^{-4} is

$$\Phi_F = e^{\overline{\ell n \Phi_F} + K_{TL} \, s_{LN}}$$

$$= e^{29.06 - (5.4)(0.27)}$$

$$= 9.7 \times 10^{11}.$$

Since $\Phi_F < \Phi_{SPEC}$ the lot can be accepted.

TABLE D-6. LM308A SAMPLE INPUT BIAS CURRENT (I_B) NEUTRON FLUENCE DEPENDENCE

Device #	I_B at neutron fluences of			Φ_F[a]	$\ln \Phi_F$
	2×10^{12} n/cm^2 (nA)	5×10^{12} n/cm^2 (nA)	1×10^{13} n/cm^2 (nA)	($\times 10^{12}$ n/cm^2)	
1	3.49	6.88	10.7	5.16	29.27
2	2.59	5.90	9.85	6.39	29.49
3	3.11	6.46	10.5	5.67	29.37
4	3.11	7.19	13.4	4.86	29.21
5	5.0	11.0	18.9	3.00	28.73
6	3.79	9.04	–	3.83	28.98
7	4.41	11.0	–	3.18	28.79
8	4.38	9.96	–	3.41	28.86
9	3.58	7.72	–	4.48	29.13
10	4.82	10.9	–	3.08	28.75
Mean	—	—	—	4.31×10^{12}	29.06
Standard Deviation	—	—	—	1.19	0.27

[a]The failure fluence Φ_F is calculated from a linear extrapolation of the I_B data to that fluence that corresponds to the application-specified failure I_B of 7 nA.

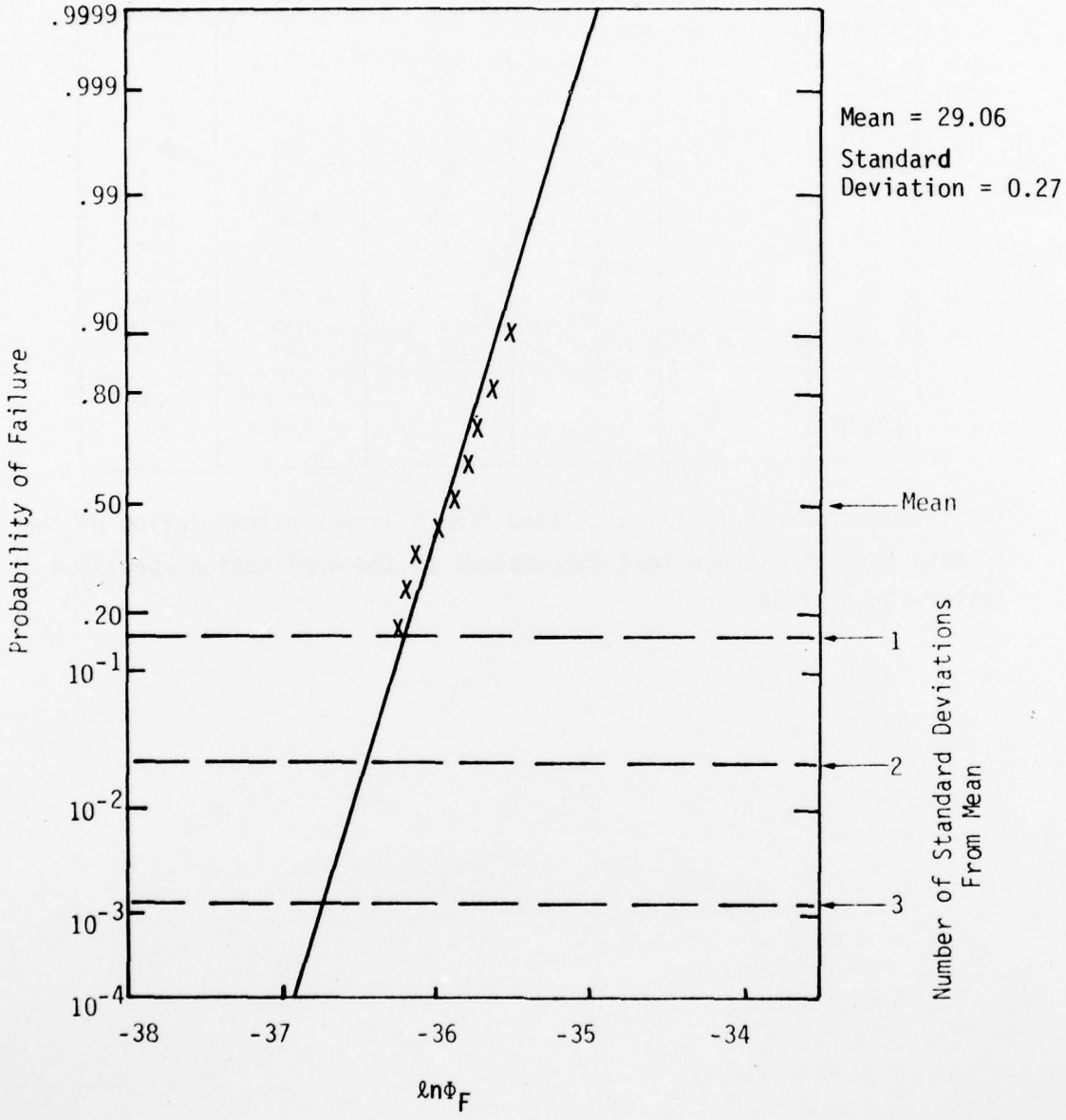

Figure D-6. LM308 natural logarithm failure fluence ($\ell n\Phi_F$) cumulative frequency distribution for an input bias current failure criterion of 7 nA.

APPENDIX E

JUNCTION FIELD-EFFECT TRANSISTOR HARDNESS ASSURANCE

E-1. EFFECTS OF NEUTRON RADIATION

The construction of a dielectrically-isolated N-channel planar-junction field-effect transistor (JFET) is shown in Figure E-1. In this device, reverse bias is applied to the gate channel depletion layer to extend it into the channel region and modulate the effective width of the conductive path between the source and the drain. The amount of reverse bias which would cause the depletion region to extend into the channel far enough to totally deplete the channel is the pinch-off voltage, V_p.

At any given gate bias where $V_G < V_p$, as the drain voltage, V_D, is increased, the drain current I_D, also increases. The ohmic voltage drop along the channel adds to the net bias across the gate-channel interface and causes the depletion region to extend further into the channel in the vicinity of the drain (see figure E-1). Consequently, when $V_D \geq (V_p - V_G)$, the space charge region which is formed at the drain end of the channel causes I_D to reach a saturation level and thus becomes insensitive to further increases in V_D.

The pinch-off voltage V_p is given by[1]

$$V_p = \frac{q\, N_D\, a^2}{8\epsilon} \qquad \text{(E-1)}$$

and the transconductance (g_m) by the approximate expression,[2]

$$g_m \cong \frac{2a\, q\, \mu\, N_D}{L} = \frac{2}{zr_{d(on)}} \qquad \text{(E-2)}$$

---

[1] W. Shedd, et al., Radiation Effects on JFET's, IEEE Trans. Nucl. Sci., NS-16, 87, December 1969.

[2] R. P. Donovan, et al., A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Lab, AFAL-TR-74-61, June 1974.

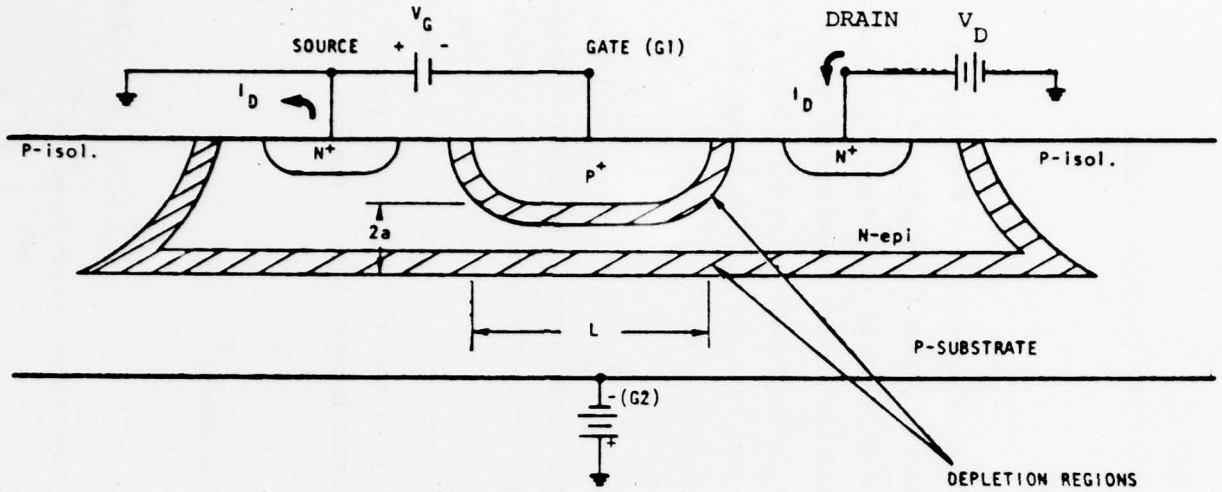

Figure E-1. Cross section of dielectrically isolated N-channel junction field-effect transistor.

where

$r_{d(on)}$ = slope of the I_{DS}-V_{DS} curve at zero gate voltage,

μ = mobility,

z = channel depth (perpendicular to the a, L plane),

a = channel width,

L = channel length,

N_D = majority carrier concentration in the channel,

q = electronic charge,

and ε = the dielectric constant.

The parameter $r_{d(on)}$ gives a measure of the resistance of the channel. The zero-gate voltage-drain saturation current, I_{DSS}, is given approximately by

$$I_{DSS} \cong \frac{g_m V_p}{3} . \qquad \text{(E-4)}$$

The most sensitive parameters to neutron damage are g_m, I_{DSS}, and V_p. g_m neutron degradation is related to the channel doping and can be characterized by[1]

$$g_{m(rad)} = g_{mo} e^{-(\frac{1}{K_J}\Phi)} \qquad \text{(E-5)}$$

where $g_{m(rad)}$ is the transconductance after irradiation, g_{mo} is the transconductance before irradiation, and K_J is $93(N_D)^{0.82}$ for an n-type channel and $398(N_D)^{0.77}$ for a p-type channel.

The effect of neutrons on JFET's is to induce carrier removal in the channel region and to reduce mobility because of traps in the gate depletion region. This leads to observed lower values for I_{DSS} and V_p.

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[1] W. Shedd, et al, Radiation Effects on JFET's, IEEE Trans. Nucl. Sci., NS-16, 87, December 1969.

Since dopant levels are usually above 10^{15} atoms/cm for planar structures, fluences of less than 10^{13} n/cm^2 would cause less than a 1% change in the carrier concentration. For heavily doped channels (about 3×10^{16} cm^2), N-channel JFET's will suffer a 50% degradation in the source to drain current at about a fluence of 2×10^{15} n/cm^2.[2] Lighter doped channels wil fail at a lower fluence. Neutron-induced damage data for P-channel JFET's is less plentiful, but there is some evidence that their neutron sensitivity is slightly better than N-channel units.

The source-to-drain current (with the gate connected to the source) I_{DSS}, decreases more rapidly with neutron radiation than g_m, which in turn decreases more rapidly than V_p. Calculated and experimental decreases of these three parameters with neutron fluence leads to the selection of I_{DSS} as the most sensitive electrical parameter for neutron effects.

E-2. CATEGORY II CRITERION

The threshold fluence (Φ_{TH}) for JFET's can be calculated from knowledge of the carrier removal rate (assume it to be 1) and the lower bound value of channel doping found in contemporary JFET's (10^{15} cm^{-3}). Using these approximate values, assuming that a 10 percent change in g_m is insignificant, and using equation E-5

$$\Phi_{TH} = -K_J \ln \frac{g_{m(rad)}}{g_{mo}}$$

$$= - \left[(93)(10^{15})^{.82}\right] \ln (.9)$$

$$= 2\times10^{13} \text{ n/cm}^2 .$$

An effective NDM, based on lot-to-lot and manufacturer-to-manufacturer variations of a JFET parameter that degrades linearly with fluence, has not been identified.

[2] R.P. Donovan, et. al, A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation, Air Force Avionics Laboratory, AFAL-TR-74-61, June 1974.

E-3. PROCUREMENT SPECIFICATION FOR HARDNESS ASSURANCE

Because the neutron degradation of important JFET parameters is related to the channel doping, HA controls are needed on channel doping. In a recent study [3], several candidate screening parameters were examined and $r_{d(on)}$ was selected as the best. An example JFET procurement specification using these proposed HA controls is given in table E-1.

TABLE E-1. EXAMPLE PROCUREMENT SPECIFICATION FOR JUNCTION FIELD-EFFECT TRANSISTORS

Hardness assurance control	Parameter	Test method	Test condition	Control level failure criterion S-2 Min	S-2 Max	S-1 Min	S-1 Max	Units
Process control	Channel doping	TBD[a]	TBD	TBD	-	TBD	-	cm^{-3}
Screen	$r_{d(on)}$[a]	TBD	$V_{GS} = 0$[a] $I_D = 0$[a]	-	TBD	-	TBD	ohms
Radiation quality conformance test	$\dot{}_F$[a]	MIL-STD-883B-1017[b]	TBD	-	-	TBD	-	mho

[a] TBD stands for to be determined, $r_{d(on)}$ is small signal drain-source on-state resistance, V_{GS} is the gate-source voltage, I_D is the drain current, and $\dot{}_F$ is the application-defined failure fluence at a given probability of failure.

[b] MIL-STD-883B is titled Test Methods and Procedures for Integrated Circuits.

[3] I. Arimura, A Study of Electronic Radiation Hardness Assurance Techniques, Air Force Weapons Laboratory, Albuquerque, NM , AFWL-TR-73-134, January 1974.

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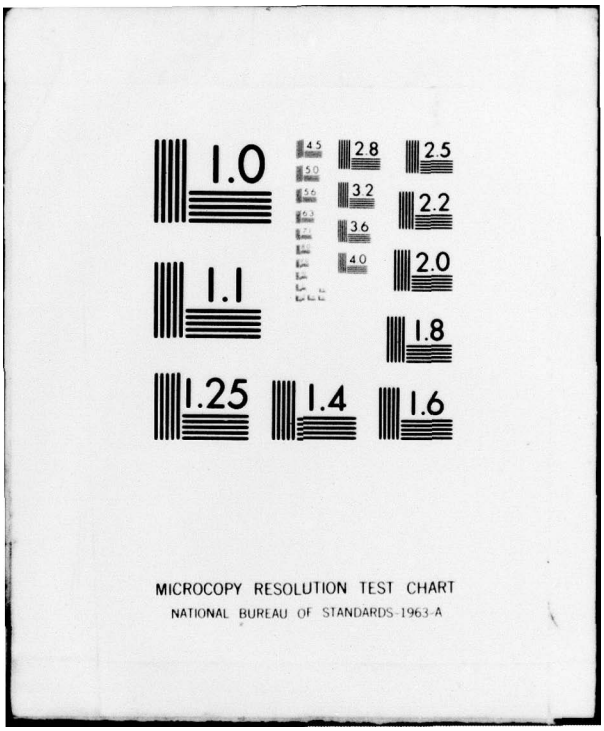
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APPENDIX F

ENVIRONMENTAL STATISTICS

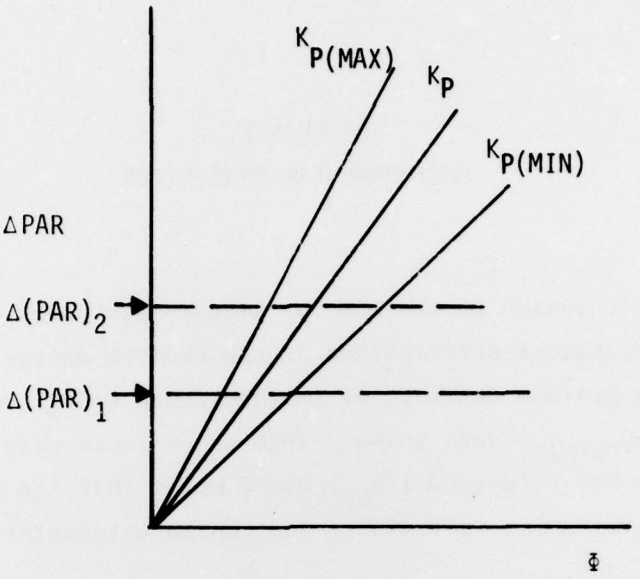
The calculation of the NDM for transistors involved the examination of the statistical distribution of the neutron damage constant (K) which yielded a minimum estimate of failure fluence (Φ_F) onece the minimum specified gain $h_{FE(MIN)}$ were known. This is an ideal case because this linear relationship between $\Delta(1/h_{FE})$ and Φ means that the $K_{D(MAX)}$ lognormal statistical distribution is scalable and can be extrapolated to low probabilities of failure.

To generalize this case with the cases which follow, call this case 1A. The case 1 designation refers to those cases where the change in electrical parameter, Δ(PAR), is linear with Φ. In this notation case 1A refers to statistically characterizing Φ at a given Δ(PAR) failure criterion and case 1B refers to statistically characterizing Δ(PAR) at a given Φ.

Case 2 refers to those situations where Δ(PAR) changes nonlinearly with Φ. Case 2A results when Φ is statistically characterized at a given Δ(PAR) failure criterion and case 2B results when Δ(PAR) is statistically characterized at a given Φ failure criterion. Case 2 is more commonly encountered than Case 1, which is unfortunate because Case 2 does not allow extrapolation to low probabilities of failure.

For case 1A (figure F-1(A)), suppose the failure criterion is given by $\Delta(PAR)_1$. The distribution of the constant of proportionality (K_p) between Δ(PAR) and Φ values due to device-to-device fabrication variations will yield a distribution in Φ. Because of the linear rela-

(a)



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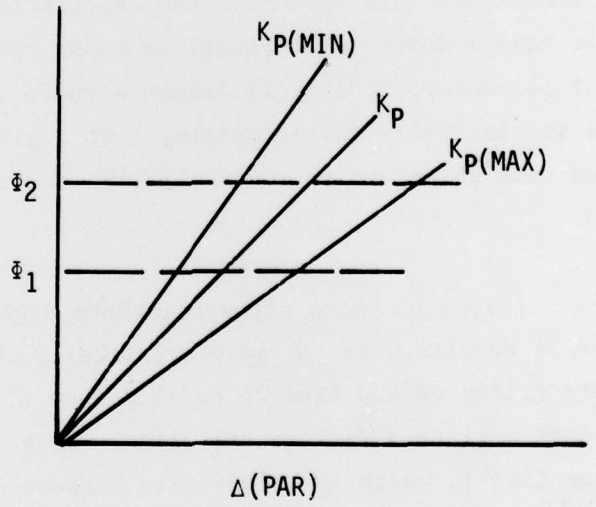


Figure F-1. Illustration of case 2 where the change in the electrical parameter Δ(PAR) is linear with neutron fluence Φ: (a) case 1A, characterizing Φ at two given Δ(PAR) failure levels, and (b) case 1B, characterizing Δ(PAR) at two given Φ failure levels. K_P is an arbitrary constant of proportionality relating Δ(PAR) and Φ.

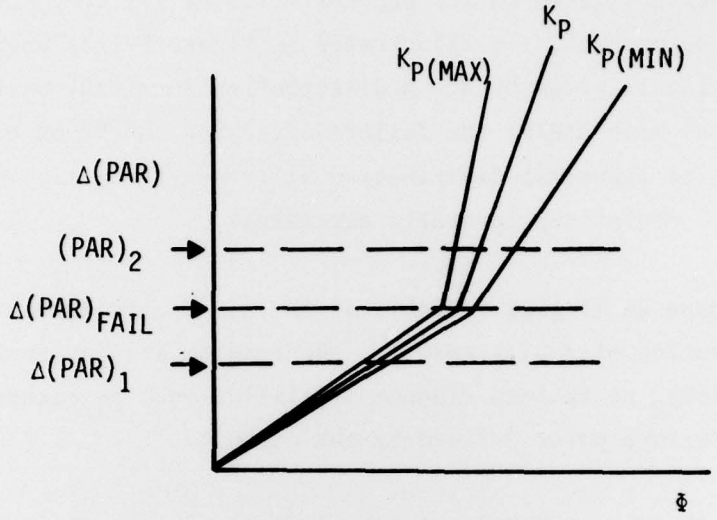
tionship between Δ(PAR) and Φ, the $K_{P(MAX)}$ lognormal statistical distribution can be extrapolated to low probabilities of failure.* The inverse of this, case 1B, is illustrated in figure F-1(B) where the failure criterion is given by Φ. A distribution in Δ(PAR) will result. When Φ is linear with Δ(PAR) the failure criterion can be on either Φ or Δ(PAR), and the lognormal distribution will have the ratios of the means to the standard deviations inversely equivalent.

For case 2A (figure F-2(A)), at the $\Delta(PAR)_1$ failure criterion, narrow distribution of Φ will result. The results are not scalable from $\Delta(PAR)_1$ to $\Delta(PAR)_2$ so failure fluence statistics must be gathered at that Δ(PAR) failure point defined by the circuit.

Case 2B (figure F-2(b)) is the inverse of case 2A in that the distribution of some parameter Δ(PAR) is gathered at some given fluence (like Φ_2). The distribution of Δ(PAR) can be shown by the points A, B, and C, where the K_p lines cross the Φ_2 line. Knowledge of the distribution at Φ_2 does not give knowledge of the distribution at Φ_1. Thus, case 2B will not yield a valid fluence margin.

Radiation lot quality conformance statistical data on category I devices (those devices which need HA controls) should, if possible, be gathered on those electrical parameters which meet case 1 criterion (Δ(PAR) is linear with Φ). The best example is the gain change $\Delta(1/h_{FE})$ for transistors. If case 1 is not possible (the critical electrical parameter does not change linearly with Φ), then case 2A should be used. For example, the procedure for reference diodes (where the reference voltage is the critical parameter and is known to change non-linearly with Φ) is to statistically characterize Φ_F at a given application-defined reference voltage failure criterion.

(a)



(b)

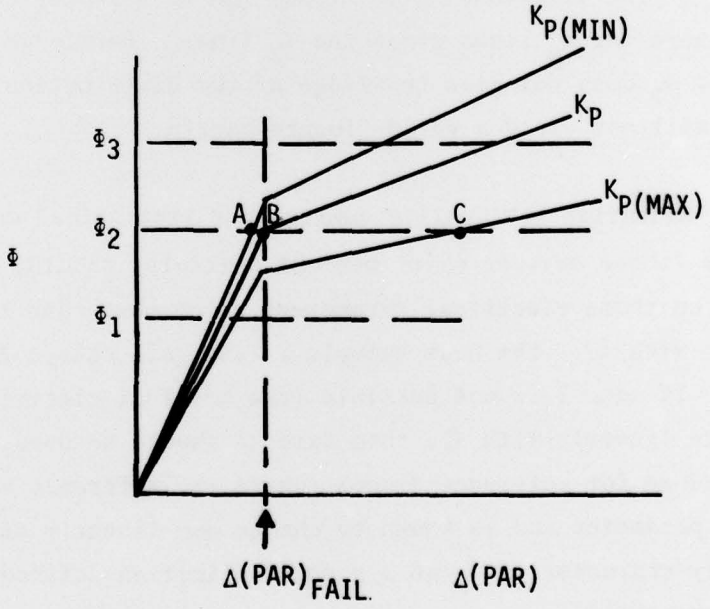


Figure F-2. Illustration of case 2 where the change in the electrical parameter Δ(PAR) is nonlinear with neutron fluence Φ: (a) case 2A, characterizing Φ at three given Δ(PAR) failure levels, and (b) case 2B, characterizing Δ(PAR) at three given Φ failure levels. K_p is an arbitrary constant of proportionality relating Δ(PAR) and Φ.

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